ines-ieee488.2

iGPIB
Hardware Manual

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Contents

1. Introduction

The iGPIB provides an interface between a microprocessor system and the GPIB specified[1] in the IEEE Std. 488.1-1987 and 488.2-1987. The controller was developed using the lastest silicon compiler technology. The iGPIB is available in several variants. The design for all variants is completely *synchronous* in order to avoid known disadvantages of the asynchronous design. In addition, GPIB bus drivers are included so it is not necessary to use additional SN 75160 and SN 75162 GPIB transceivers.[2]

1.1. iGPIB 9914

Fully hard and software compatible with Texas Instruments TMS 9914 A. Available in 40 pin DIL and 44 pin PLCC design. This variant may be used as replacement for the original TMS 9914 A in existing hardware designs.

1.2. iGPIB 7210

Fully hard and software compatible with NEC µPD 7210 C. Available in 40 pin DIL design. This variant may be used as replacement for the original NEC µPD 7210 C in existing hardware designs. In addition to the NEC 7210 functionallity the controller can be switched into the extended iGPIB mode by software.

1.3. iGPIB 72010 ISA

Software compatible with NEC µPD 7210 C in initial state. In addition to the NEC 7210 functionallity the controller can be switched into the extended iGPIB mode by software. Available in 80 pin TQFP design. This variant includes a complete ISA Interface which allows a 'one chip design' for GPIB ISA boards.

1.4. iGPIB 72010 PCMCIA

Software compatible with NEC µPD 7210 C in initial state. In addition to the NEC 7210 functionallity the controller can be switched into the extended iGPIB mode by software. Available in 80 pin TQFP design. This variant includes a complete PCMCIA Interface which allows a 'one chip design' for GPIB PCMCIA cards.

If using the iGPIB as replacement for the TMS9914 or NEC 7210, please refer to the original documentation of these controllers. This document describes the iGPIB controller in extended mode.

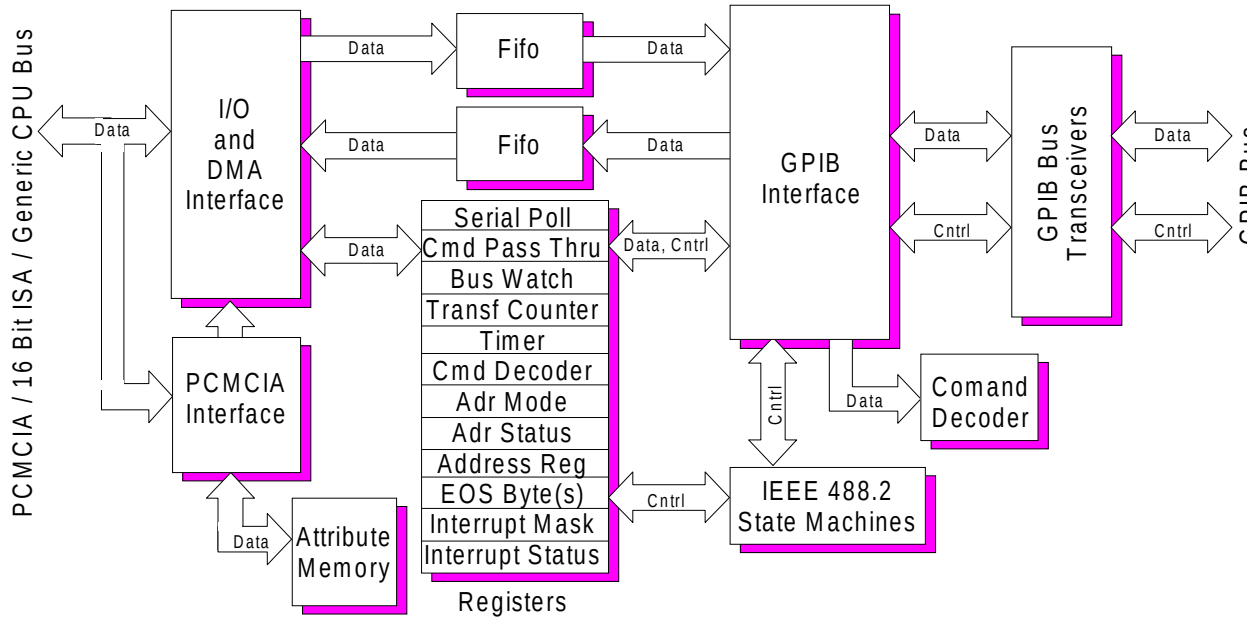
2. Features

- All IEEE488.1 interface function are provided:
  - Source Handshake (SH1)
  - Acceptor Handshake (AH1)
  - Talker or Extended Talker (T5 or TE5)
  - Listener or Extended Listener (L3 or LE3)
  - Service Request (SR1)
  - Remote/Local (RL1)
  - Parallel Poll
    remote configuration(PP1), local configuration (PP2)
  - Device Clear (DC1), Device Trigger (DT1)
  - Controller, all capabilities (C 1,2,3,4,5).
- Software compatible with the NEC µPD 7210 C GPIB controller. Hardware compatible, if using the 40-pin DIL version.

[1]The GPIB is the General Purpose Interface Bus. The system was invented by Hewlett-Parkard in the 1960´s. Now, the GPIB is defined by international standards, IEEE488 and IEC625, respectively. Throughout this paper, the term GPIB always refers to the bus as specified in IEEE488.
[2] Actually the bus drivers are included only in the 80 TQFP designs, in the next generation (avaliable November 1998) the drivers will be included in all variants.

- Two 255 byte FIFO memories on chip. May be used as IEEE488.2 input/output queues in device operation or as transfer buffers in Controller[3] operation. Complete hardware support for the implementation of an IEEE488.2 Message Exchange Control.
- 30 MHz clock rate in TQFP80 design. 4 / 8 / 30 MHz[4] clock rate in DIL40 design. T1 delays of 2000, 1100, 700, 500, 350 and 250 ns programmable. Supports all IEEE488.1 timers in hardware, even T8 (100 µs). No software timers required.
- Meets all requirements of IEEE488.2-1987
  - Bus line monitoring
  - Preferred request service implementation
  - Does not source any data without Listeners
  - Listener function disable
  - Supports up to three EOS messages and four handshake holdoff conditions.
- Two DMA modes: asynchronous (NEC µPD 7210 C) and sychronous (high-speed). Supports 16, 32 and 64 bit wide DMA data paths at max. 30 MByte/sec.
- 16-bit timeout counter with 1 ms resolution.
- 16-bit data transfer counter with automatic EOI generation (talk) and automatic RFD holdoff (listen).
- Build in GPIB bus transceivers.

3. Block Diagram



[3] We use "Controller" for the IEEE488.1 CONTROLLER operation, whereas "controller" denotes a microprocessor peripherial interfacing to the GPIB.

[4] The actual generation uses 30 MHz for all variants. In the next generation (available November 1998) the iGPIB 9914 DIL40 and PLCC44 will use 4 MHz, the iGPIB 7210 DIL40 will use 8 MHz and all other variants will use 30 MHz.

4. Pin Descriptions

4.1.Pin Description i7210 (40 DIP) & i72010 (68 PLCC)

No. PLCC 68	No. DIP 40	Name	Function	Active	Group	Type
1		GND	Ground		PWR	
2	1	T/R1	Controls direction of DIO0~-DIO7~, DAV~, NRFD~ and NDAC~	1=in	TRCTL	O
3		DMADB3	Synchronous DMA Data Bus	high	DMADB	I/O
4	2	T/R2	Function programmable via the address-mode register		TRCTL	O
5	3	CLOCK	30 MHz clock or 8 MHz clock			I
6		DMADB4	Synchronous DMA Data Bus	high	DMADB	I/O
7	4	RESET	Reset of all internal registers, flip-flops and functions	high	SCTL	I
8		DMADB5	Synchronous DMA Data Bus	high	DMADB	I/O
9	5	T/R3	Function programmable via the address-mode register		TRCTL	O
10	6	DMAREQ	Request of a DMA cycle	high	DCTL	O
11		DMADB6	Synchronous DMA Data Bus	high	DMADB	I/O
12	7	DMAACK~	DMA acknowledge	low	DCTL	I
13		DMADB7	Synchronous DMA Data Bus	high	DMADB	I/O
14	8	CS~	Enables register access	low	CPUCTL	I
15	9	RD~	Indicates read register access	low	CPUCTL	I
16		Vcc	+5V		PWR	
17	10	WR~	Indicates write register access	low	CPUCTL	I
18		GND	Ground		PWR	
19	11	INT	OR of all unmasked and active interrupt conditions	select.	MISC	O
20		CLKSEL	high: external 8MHz NEC 7210 compatible, low: external 30MHz clock, at CLOCK input	-	MISC	I
21	12	D0	CPU Data Bus	high	CPUDB	I/O
22	13	D1	CPU Data Bus	high	CPUDB	I/O
23		CIC~	iGPIB is Controller in Charge	low	TRCTL	I/O
24	14	D2	CPU Data Bus	high	CPUDB	I/O
25		RS4	Register select	high	CPUCTL	I
26	15	D3	CPU Data Bus	high	CPUDB	I/O
27	16	D4	CPU Data Bus	high	CPUDB	I/O
28		SC	iGPIB is System Controller (SCAS)	high	TRCTL	O
29	17	D5	CPU Data Bus	high	CPUDB	I/O
30		AUXI	Auxiliary input	low	MISC	I
31	18	D6	CPU Data Bus	high	CPUDB	I/O
32	19	D7	CPU Data Bus	high	CPUDB	I/O
33		DISC	Disable Controller, pull to GND	high	MISC	I
34	20	GND	Ground		PWR	
35		Vcc	+5V		PWR	
36	21	RS0	Register Select	high	CPUCTL	I
37		DMA_X	Synchronous DMA active	high	DCTL	O
38	22	RS1	Register select	high	CPUCTL	I

39		SE~	Internal use only, do not connect (Boundary Scan Enable)	low		I
40	23	RS2	Register Select	high	CPUCTL	I
41	24	IFC~	Interface Clear	low	GCTL	I/O
42		RS4	Register Select	high	CPUCTL	I
43	25	REN~	Remote Enable	low	GCTL	I/O
44	26	ATN~	Attention	low	GCTL	I/O
45		XDMATLK	Determines direction for sync. DMA Transfers	high	DCTL	O
46	27	SRQ~	Service Request	low	GCTL	I/O
47		AUX_O	Auxiliary output	high	MISC	O
48	28	DIO1~	GPIB Data Bus	low	GDIO	I/O
49	29	DIO2~	GPIB Data Bus	low	GDIO	I/O
50						
51	30	DIO3~	GPIB Data Bus	low	GDIO	I/O
52		GND	Ground		PWR	
53	31	DIO4~	GPIB Data Bus	low	GDIO	I/O
54		Vcc	+5V		PWR	
55	32	DIO5~	GPIB Data Bus	low	GDIO	I/O
56	33	DIO6~	GPIB Data Bus	low	GDIO	I/O
57						
58	34	DIO7~	GPIB Data Bus	low	GDIO	I/O
59		PE	Parallel Poll Enable for 3-State drivers		TRCTL	O
60	35	DIO8~	GPIB Data Bus	low	GDIO	I/O
61	36	DAV~	Data Valid, handshake line	low	GCTL	I/O
62		DMADB0	Synchronous DMA Data Bus	high	DMADB	I/O
63	37	NRFD~	Not Ready for Data, handshake line	low	GCTL	I/O
64		DMADB1	Synchronous DMA Data Bus	high	DMADB	I/O
65	38	NDAC~	Not Data Accepted, handshake line	low	GCTL	I/O
66	39	EOI~	End Or Identify, indicates transfer end or parallel poll	low	GCTL	I/O
67		DMADB2	Synchronous DMA Data Bus	high	DMADB	I/O
68	40	Vcc	+5V		PWR	

4.2.Pin Description i9914 (40 DIP + 44 PLCC)

Pin-No. PLCC44	Pin-No. DIL40	Name	Function	Active	Group	Type
1	-	GND	Ground			
2	1	ACCRQ~	DMA Request	low	CPU	Out, 4 mA
3	2	ACCGR~	DMA Acklowledge	low	CPU	In
4	3	CE~	Chip Enable	low	CPU	In
5	4	WE~	Write Enable	low	CPU	In
6	5	DBIN	Databus Enable to Input	high	CPU	In
7	6	RS0	Address line 0	high	CPU	In
8	7	RS1	Address line 1	high	CPU	In
9	8	RS2	Address line 2	high	CPU	In
10	9	INT~	Interrupt	low	CPU	Out, open drain, 4 mA
11	10	D7	Data bus line 7 (LSB!)	high	CPU	Bidir, 4 mA
12	11	D6	Data bus line 6	high	CPU	Bidir, 4 mA
13	12	D5	Data bus line 5	high	CPU	Bidir, 4 mA
14	13	D4	Data bus line 4	high	CPU	Bidir, 4 mA
15	14	D3	Data bus line 3	high	CPU	Bidir, 4 mA
16	15	D2	Data bus line 2	high	CPU	Bidir, 4 mA
17	16	D1	Data bus line 1	high	CPU	Bidir, 4 mA
18						
19	17	D0	Data bus line 0 (MSB!)	high	CPU	Bidir, 4 mA
20	18	0~	Clock			In
21	19	RESET~	Chip reset	low	CPU	In
22	20	GND	Ground			
23	21	TE	Talker enabled	high		Out, 4 mA
24	22	REN	Remote enable (GPIB-Line)	low	GPIB	Bidir, 4 mA
25	23	IFC	Interface clear (GPIB-Line)	low	GPIB	Bidir, 4 mA
26	24	NDAC	Not data accepted (GPIB-Line)	low	GPIB	Bidir, 4 mA
27	25	NRFD	Not ready for data (GPIB-Line)	low	GPIB	Bidir, 4 mA
28						
29	26	DAV	Data valid (GPIB-Line)	low	GPIB	Bidir, 4 mA
30	27	EOI	End or identify (GPIB-Line)	low	GPIB	Bidir, 4 mA
31	28	ATN	Attention (GPIB-Line)	low	GPIB	Bidir, 4 mA
32	29	SRQ	Service request (GPIB-Line)	low	GPIB	Bidir, 4 mA
33	30	CONT~	Device is controller in charge	low		
34	31	DIO8	GPIB data line 8	low	GPIB	Bidir, 4 mA
35	32	DIO7	GPIB data line 7	low	GPIB	Bidir, 4 mA
36	33	DIO6	GPIB data line 6	low	GPIB	Bidir, 4 mA
37	34	DIO5	GPIB data line 5	low	GPIB	Bidir, 4 mA
38	35	DIO4	GPIB data line 4	low	GPIB	Bidir, 4 mA
39	36	DIO3	GPIB data line 3	low	GPIB	Bidir, 4 mA
40						
41	37	DIO2	GPIB data line 2	low	GPIB	Bidir, 4 mA
42	38	DIO1	GPIB data line 1	low	GPIB	Bidir, 4 mA
43	39	TR	Trigger	high		Out, 4 mA
44	40	Vcc	Power			

4.3.Pin Description i-D-72010 (80 QFP)

Pin-No. i D 72010	Name	Function	Active	Group	Type
1	Vcc	+5V	-		
2	ATN~	attention	low	GPIB	Bidir, 4 mA
3	DMA_O	Determines direction for DMA Transfers	high	CPU	Out, 6 mA
4	SRQ~	service request	low	GPIB	Bidir, 4 mA
5	AUX_O	auxiliary output	high		Out, 6 mA
6	DIO1~	GPIB data line 1	low	GPIB	Bidir, 4 mA
7	DIO2~	GPIB data line 2	low	GPIB	Bidir, 4 mA
8	PACK	RS0..RS4 chip adressing mode high: 3 bit addressing, 7210 mode, only RS0..RS2 are valid, bank switch necessary to access all registers. low: 5 bit addressing, RS0..RS4 are valid, all 32 registers can be accessed	-		In, PU 100k
9	DIO3~	GPIB data line 3	low	GPIB	Bidir, 4 mA
10	GND	ground	-		
11	DRV_ENA~	high: Internal GPIB line drivers disabled low: Internal GPIB line drivers enabled	low		In, PU 100k
12	DIO4~	GPIB data line 4	low	GPIB	Bidir, 4 mA
13	Vcc	+5V	-		
14	DIO5~	GPIB data line 5	low	GPIB	Bidir, 4 mA
15	DIO6~	GPIB data line 6	low	GPIB	Bidir, 4 mA
16	FIFOTEST~	Internal use only, do not connect (Fifo test Enable)	low		In, PU 100k
17	DIO7~	GPIB data line 7	low	GPIB	Bidir, 4 mA
18	PE	parallel poll enable for 3-state drivers	high		Out, 6 mA
19	DIO8~	GPIB data line 8	low	GPIB	Bidir, 4 mA
20	Vcc	+5V	-		
21	GND	ground	-		
22	DAV~	data valid	low	GPIB	Bidir, 4 mA
23	DMADB0	synchronous DMA data bus	high	CPU	Bidir, 24 mA
24	NRFD~	not ready for data, handshake line	low	GPIB	Bidir, 4 mA
25	DMADB1	synchronous DMA data bus	high	CPU	Bidir, 24 mA
26	NDAC~	not data accepted handshake line	low	GPIB	Bidir, 4 mA
27	EOI~	end or identify (GPIB line)	low	GPIB	Bidir, 4 mA
28	DMADB2	synchronous DMA data bus	high	CPU	Bidir, 24 mA
29	Vcc	+5V	-		
30	GND	ground	-		
31	PCMCIA~	PCMCIA mode	low		In, PU 100k
32	T/R1	controls direction of DIO1~ - DIO8, DAV~, NRFD~ and NDAC~	1=in		Out, 6 mA
33	DMADB3	synchronous DMA data bus	high	CPU	Bidir, 24 mA
34	T/R2	function programmable via address-mode register	-		Out, 6 mA
35	CLOCK	clock	-		In, PU 100k
36	DMADB4	synchronous DMA data bus	high	CPU	Bidir, 24 mA
37	RESET	reset of all internal registers, flip-flops and functions	high	CPU	In

38	DBADB5	synchronous DMA data bus	high	CPU	Bidir, 24 mA
39	T/R3	function programmable via adress-mode register	-		Out, 6 mA
40	GND	ground	-		
41	Vcc	+5V	-		
42	DMAREQ	request of DMA cycle	high	CPU	Out, 24 mA
43	DMADB6	synchronous DMA data bus	high	CPU	Bidir, 24 mA
44	DMAACK~	DMA acknoledge	low	CPU	In
45	DMADB7	synchronous DMA data bus	high	CPU	Bidir, 24 mA
46	CS~	enables register access	low	CPU	In
47	RD~	indicates read access to register	low	CPU	In, PU 100k
48	Vcc	+5V	-		
49	WR~	indicates write access to register	low	CPU	In, PU 100k
50	GND	ground	-		
51	CLKOUT				Out, 6 mA
52	INT	OR of all unmasked and active interrupt conditions	select.	CPU	Out, 24 mA
53	CLKSEL	high: external 8MHz NEC 7210 compatible, low: external 30MHz clock, at CLOCK input	-		In, PU 100k
54	D0	CPU data bus line 0	high	CPU	Bidir, 24 mA
55	D1	CPU data bus line 1	high	CPU	Bidir, 24 mA
56	CIC	controller in charge	high		Out, 24 mA
57	D2	CPU data bus line 2	high	CPU	Bidir, 24 mA
58	RS4	register select	high	CPU	In, PU 100k
59	D3	CPU data bus line 3	high	CPU	Bidir, 24 mA
60	GND	ground	-		
61	Vcc	+5V	-		
62	D4	CPU data bus line 4	high	CPU	Bidir, 24 mA
63	SC	iGPIB is system controller (SCAS)	high		Out, 6 mA
64	D5	CPU data bus line 5	high	CPU	Bidir, 24 mA
65	SCSEL	reflected by SCSEL bit in Extended Status register	-		In, PU 100k
66	D6	CPU data bus line 6	high	CPU	Bidir, 24 mA
67	D7	CPU data bus line 7	high	CPU	Bidir, 24 mA
68	DISC	disable controller	high		In, PD 100k
69	GND	ground	-		
70	Vcc	+5V	-		
71	ISA~	ISA Mode	low		In, PU 100k
72	RS0	register select	high	CPU	In, PU 100k
73	DMA_X	synchronous DMA active	high	CPU	Out, 6 mA
74	RS1	register select	high	CPU	In, PU 100k
75	SE~	Internal use only, do not connect (Boundary Scan Enable)	-		In, PU 100k
76	RS2	register select	high	CPU	In, PU 100k
77	IFC~	interface clear	low	GPIB	Bidir, 4 mA
78	RS3	register select	high	CPU	In, PU 100k
79	REN~	remote enable	low	GPIB	Bidir, 4 mA
80	GND	ground	-		

4.4.Pin Description i-ISA-72010 (80 QFP)

Pin-No. i ISA 72010	Name	Function	Active	Group	Type
1	Vcc	+5V	-		
2	ATN~	attention	low	GPIB	Bidir, 4 mA
3	DB_ENL~	ISA databus enable lower byte	low		Out, 6 mA
4	SRQ~	service request	low	GPIB	Bidir, 4 mA
5	DB_ENH~	ISA databus enable higher byte	low		Out, 6 mA
6	DIO1~	GPIB data line 1	low	GPIB	Bidir, 4 mA
7	DIO2~	GPIB data line 2	low	GPIB	Bidir, 4 mA
8	PACK	RS0..RS4 chip adressing mode high: 3 bit addressing, 7210 mode, only RS0..RS2 are valid, bank switch necessary to access all registers. low: 5 bit addressing, RS0..RS4 are valid, all 32 registers can be accessed	-		In, PU 100k
9	DIO3~	GPIB data line 3	low	GPIB	Bidir, 4 mA
10	GND	ground	-		
11	DRV_ENA~	high: Internal GPIB line drivers disabled low: Internal GPIB line drivers enabled	low		In, PU 100k
12	DIO4~	GPIB data line 4	low	GPIB	Bidir, 4 mA
13	Vcc	+5V	-		
14	DIO5~	GPIB data line 5	low	GPIB	Bidir, 4 mA
15	DIO6~	GPIB data line 6	low	GPIB	Bidir, 4 mA
16	FIFOTEST~	Internal use only, do not connect (Fifo test Enable)	low		In, PU 100k
17	DIO7~	GPIB data line 7	low	GPIB	Bidir, 4 mA
18	PE	parallel poll enable for 3-state drivers	high		Out, 6 mA
19	DIO8~	GPIB data line 8	low	GPIB	Bidir, 4 mA
20	Vcc	+5V	-		
21	GND	ground	-		
22	DAV~	data valid	low	GPIB	Bidir, 4 mA
23	AT_SD8	CPU data bus 8	high	CPU	Bidir, 24 mA
24	NRFD~	not ready for data, handshake line	low	GPIB	Bidir, 4 mA
25	AT_SD9	CPU data bus 9	high	CPU	Bidir, 24 mA
26	NDAC~	not data accepted handshake line	low	GPIB	Bidir, 4 mA
27	EOI~	end or identify (GPIB line)	low	GPIB	Bidir, 4 mA
28	AT_SD10	CPU data bus 10	high	CPU	Bidir, 24 mA
29	Vcc	+5V	-		
30	GND	ground	-		
31	PCMCIA~	PCMCIA mode	low		In, PU 100k
32	T/R1	controls direction of DIO1~ - DIO8, DAV~, NRFD~ and NDAC~	1=in		Out, 6 mA
33	AT_SD11	CPU data bus 11	high	CPU	Bidir, 24 mA
34	T/R2	function programmable via address-mode register	-		Out, 6 mA
35	CLOCK	clock	-		In, PU 100k
36	AT_SD12	CPU data bus 12	high	CPU	Bidir, 24 mA

37	AT_RESET	reset of all internal registers, flip-flops and functions	high	CPU	In
38	AT_SD13	CPU data bus 13	high	CPU	Bidir, 24 mA
39	T/R3	function programmable via adress-mode register	-		Out, 6 mA
40	GND	ground	-		
41	Vcc	+5V	-		
42	AT_DRQ	request of DMA cycle	high	CPU	Out, 24 mA
43	AT_SD14	CPU data bus 14	high	CPU	Bidir, 24 mA
44	AT_DACK~	DMA acknoledge	low	CPU	In
45	AT_SD15	CPU data bus 15	high	CPU	Bidir, 24 mA
46	CS~	enables register access	low	CPU	In
47	AT_IOR~	indicates read access to register	low	CPU	In, PU 100k
48	Vcc	+5V	-		
49	AT_IOW~	indicates write access to register	low	CPU	In, PU 100k
50	GND	ground	-		
51	CLKOUT				Out, 6 mA
52	AT_IRQ	OR of all unmasked and active interrupt conditions	select.		Out, 24 mA
53	CLKSEL	high: external 8MHz NEC 7210 compatible, low: external 30MHz clock, at CLOCK input	-		In, PU 100k
54	AT_SD0	CPU data bus line 0	high	CPU	Bidir, 24 mA
55	AT_SD1	CPU data bus line 1	high	CPU	Bidir, 24 mA
56	CIC	iGPIB controller in charge	high		Out, 24 mA
57	AT_SD2	CPU data bus line 2	high	CPU	Bidir, 24 mA
58	AT_SA4	register select	high	CPU	In, PU 100k
59	AT_SD3	CPU data bus line 3	high	CPU	Bidir, 24 mA
60	GND	ground	-		
61	Vcc	+5V	-		
62	AT_SD4	CPU data bus line 4	high	CPU	Bidir, 24 mA
63	SC	iGPIB is system controller (SCAS)	high		Out, 6 mA
64	AT_SD5	CPU data bus line 5	high	CPU	Bidir, 24 mA
65	SCSEL	reflected by SCSEL bit in Extended Status register	-		In, PU 100k
66	AT_SD6	CPU data bus line 6	high	CPU	Bidir, 24 mA
67	AT_SD7	CPU data bus line 7	high	CPU	Bidir, 24 mA
68	DISC	disable controller	high		In, PD 100k
69	GND	ground	-		
70	Vcc	+5V	-		
71	ISA~	ISA Mode	low		In, PU 100k
72	AT_SA0	register select	high	CPU	In, PU 100k
73	DT_R~	ISA data bus direction	low	CPU	Out, 6 mA
74	AT_SA1	register select	high	CPU	In, PU 100k
75	SE~	Internal use only, do not connect (Boundary Scan Enable)	low		In, PU 100k
76	AT_SA2	register select	high	CPU	In, PU 100k
77	IFC~	interface clear	low	GPIB	Bidir, 4 mA
78	AT_SA3	register select	high	CPU	In, PU 100k
79	REN~	remote enable	low	GPIB	Bidir, 4 mA
80	GND	ground	-		

4.5.Pin Description i-PC-72010 (80 QFP)

Pin-No. i PC 72010	Name	Function	Active	Group	Type
1	Vcc	+5V	-		
2	ATN~	attention	low	GPIB	Bidir, 4 mA
3	EECS	EEPROM select	high		Out, 6 mA
4	SRQ~	service request	low	GPIB	Bidir, 4 mA
5	EECK	synchronous clock 4 µs	-		Out, 6 mA
6	DIO1~	GPIB data line 1	low	GPIB	Bidir, 4 mA
7	DIO2~	GPIB data line 2	low	GPIB	Bidir, 4 mA
8	PACK	RS0..RS4 chip adressing mode high: 3 bit addressing, 7210 mode, only RS0..RS2 are valid, bank switch necessary to access all registers. low: 5 bit addressing, RS0..RS4 are valid, all 32 registers can be accessed	-		In, PU 100k
9	DIO3~	GPIB data line 3	low	GPIB	Bidir, 4 mA
10	GND	ground	-		
11	DRV_ENA~	high: Internal GPIB line drivers disabled low: Internal GPIB line drivers enabled	low		In, PU 100k
12	DIO4~	GPIB data line 4	low	GPIB	Bidir, 4 mA
13	Vcc	+5V	-		
14	DIO5~	GPIB data line 5	low	GPIB	Bidir, 4 mA
15	DIO6~	GPIB data line 6	low	GPIB	Bidir, 4 mA
16	FIFOTEST~	Internal use only, do not connect (Fifo test Enable)	low		In, PU 100k
17	DIO7~	GPIB data line 7	low	GPIB	Bidir, 4 mA
18	PE	parallel poll enable for 3-state drivers	high		Out, 6 mA
19	DIO8~	GPIB data line 8	low	GPIB	Bidir, 4 mA
20	Vcc	+5V	-		
21	GND	ground	-		
22	DAV~	data valid	low	GPIB	Bidir, 4 mA
23	PA5	PCMCIA address bus 5		PCM	In
24	NRFD~	not ready for data, handshake line	low	GPIB	Bidir, 4 mA
25	PA6	PCMCIA address bus 6		PCM	In
26	NDAC~	not data accepted handshake line	low	GPIB	Bidir, 4 mA
27	EOI~	end or identify (GPIB line)	low	GPIB	Bidir, 4 mA
28	PA7	PCMCIA address bus 7		PCM	In
29	Vcc	+5V	-		
30	GND	ground	-		
31	PCMCIA~	PCMCIA mode	low		In, PU 100k
32	T/R1	controls direction of DIO1~ - DIO8, DAV~, NRFD~ and NDAC~	1=in		Out, 6 mA
33	PA8	PCMCIA address bus 8		PCM	In
34	T/R2	function programmable via address-mode register	-		Out, 6 mA
35	CLOCK	clock	-		In, PU 100k
36	PA9	PCMCIA address bus 9			In

37	RESET	reset of all internal registers, flip-flops and functions	high	PCM	In
38	NCE2~	chip select odd address	low	PCM	In
39	T/R3	function programmable via adress-mode register	-		Out, 6 mA
40	GND	ground	-		
41	Vcc	+5V	-		
42	NINPACK	indicates IO-read-access to configured address range	low	PCM	Out, 24 mA
43	NWE~	write enable for attribute memory	low	PCM	In
44	VPP1	programming voltage to program EEPROM			In
45	EEDO	serial data line from EEPROM	high		In
46	NCE1~	chip select even address	low	PCM	In
47	NIORD~	read enable for IO address range	low	PCM	In, PU 100k
48	Vcc	+5V	-		
49	NIOWR~	write anable for IO address range	low	PCM	In, PU 100k
50	GND	ground	-		
51	PWRDWN			PCM	Out, 6 mA
52	NIREQ~	interrupt	low	PCM	Out, 24 mA
53	CLKSEL	high: external 8MHz NEC 7210 compatible, low: external 30MHz clock, at CLOCK input	-		In, PU 100k
54	PD0	PCMCIA data bus 0	high	PCM	Bidir, 24 mA
55	PD1	PCMCIA data bus 1	high	PCM	Bidir, 24 mA
56	NOE~	read enable for attribute memory	low	PCM	In
57	PD2	PCMCIA data bus 2	high	PCM	Bidir, 24 mA
58	PA4	PCMCIA address bus 4	high	PCM	In, PU 100k
59	PD3	PCMCIA data bus 3	high	PCM	Bidir, 24 mA
60	GND	ground	-		
61	Vcc	+5V	-		
62	PD4	PCMCIA data bus 4	high	PCM	Bidir, 24 mA
63	SC	iGPIB is system controller (SCAS)	low		Out, 6 mA
64	PD5	PCMCIA data bus 5	high	PCM	Bidir, 24 mA
65	NREG~	low indicates access to attribute memory or IO-address range	low	PCM	In, PU 100k
66	PD6	PCMCIA data bus 6	high	PCM	Bidir, 24 mA
67	PD7	PCMCIA data bus 7	high	PCM	Bidir, 24 mA
68	DISC	disable controller	high		In, PD 100k
69	GND	ground	-		
70	Vcc	+5V	-		
71	ISA~	ISA Mode	low		In, PU 100k
72	PA0	PCMCIA address bus 0	high	PCM	In, PU 100k
73	EEDI~	serial data line to EEPROM	high		Out, 6 mA
74	PA1	PCMCIA address bus 1	high	PCM	In, PU 100k
75	SE~	Internal use only, do not connect (Boundary Scan Enable)	low		In, PU 100k
76	PA2	PCMCIA address bus 2	high	PCM	In, PU 100k
77	IFC~	interface clear	low	GPIB	Bidir, 4 mA
78	PA3	PCMCIA address bus 3	high	PCM	In, PU 100k
79	REN~	remote enable	low	GPIB	Bidir, 4 mA
80	GND	ground	-		

5. Register Set

The iGPIB provides 44 registers (24 write/20 read). In the *NEC compatible mode*, only the lower 8 registers can be accessed and the RS3 and RS4 address inputs are ignored.

D7	D6	D5	D4	D3	D2	D1	D0	Adr.(HEX)	R/W	Name
D7	D6	D5	D4	D3	D2	D1	D0	0	R	Data In
B7	B6	B5	B4	B3	B2	B1	B0	0	W	Byte Out
CPT	APT	DET	END	DEC	ERR	DO	DI	1	R	Interrupt Status 1
CPT	APT	DET	END	DEC	ERR	DO	DI	1	W	Interrupt Mask 1
INT	SRQI	LOK	REM	CO	LOKC	REMC	ADSC	2	R	Interrupt Status 2
0	SRQI	DMAO	DMAI	CO	LOKC	REMC	ADSC	2	W	Interrupt Mask 2
S8	PEND	S6	S5	S4	S3	S2	S1	3	R	Serial Poll Status
S8	rsv	S6	S5	S4	S3	S2	S1	3	W	Serial Poll Mode
CIC	ATN	SPMS	LPAS	TPAS	LA	TA	MJMN	4	R	Address Status
ton	lon	TRM1	TRM0	IFENA	OFENA	ADM1	ADM0	4	W	Address Mode
CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0	5	R	Command Pass Through
CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0	5	W	Auxiliary Registers
T8RUN	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0	6	R	Address 0
ARS	DT	DL	AD5	AD4	AD3	AD2	AD1	6	W	Address 0/1
EOI	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1	7	R	Address 1
EOS7	EOS6	EOS5	EOS4	EOS3	EOS2	EOS1	EOS0	7	W	EOS
OF_WM	IF_WM	OFRDY	IFRDY	OF_EM	IF_FL	OF_WM	IF_WM	8	R	FIFO Status
				AUX_O	DMA_S	DMA_X	DMA_O	8	W	XDMA Control
	FF_ERR	ATN	IFC	TCT	CMD	TC	TMO	9	R	Interrupt Status 3
	FF_ERR	ATN	IFC	TCT	CMD	TC	TMO	9	W	Interrupt Mask 3
OF_WM	IF_WM	OFRDY	IFRDY	OF_EM	IF_FL	OF_WM	IF_WM	A	R	Interrupt Status 4
OF_WM	IF_WM	OFRDY	IFRDY	OF_EM	IF_FL	OF_WM	IF_WM	A	W	Interrupt Mask 4
TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0	B	R	TC lower byte
TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0	B	W	TC lower byte
TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8	C	R	TC upper byte
TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8	C	W	TC upper byte
REVC7	REVC6	REVC5	REVC4	REVC3	REVC2	REVC1	REVC0	D	R	Revision Code
TMO7	TMO6	TMO5	TMO4	TMO3	TMO2	TMO1	TMO0	D	W	TMO lower byte
OEM7	OEM6	OEM5	OEM4	OEM3	OEM2	OEM1	OEM0	E	R	OEM Code
TMO15	TMO14	TMO13	TMO12	TMO11	TMO10	TMO9	TMO8	E	W	TMO upper byte
			OF_FL	IF_EM	LIDIS	AUXIN	OQMU	F	R	Extended Status
TC_LBH	TC_TLK	TC_ENA	EOIDIS	E2ENA	E1ENA	MAVEN	TRGEN	F	W	Extended Mode
IFC7	IFC6	IFC5	IFC4	IFC3	IFC2	IFC1	IFC0	10	R	Input FIFO Count
IFW7	IFW6	IFW5	IFW4	IFW3	IFW2	IFW1	IFW0	10	W	Input FIFO watermark
OFC7	OFC6	OFC5	OFC4	OFC3	OFC2	OFC1	OFC0	11	R	Output FIFO count
OFW7	OFW6	OFW5	OFW4	OFW3	OFW2	OFW1	OFW0	11	W	Output FIFO watermark
DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	12	R	Bus Data Monitor
DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	12	W	Bus Data Monitor
EOI	REN	SRQ	ATN	IFC	NDAC	NRFD	DAV	13	R	Bus Ctrl Monitor
EOI	REN	SRQ	ATN	IFC	NDAC	NRFD	DAV	13	W	Bus Ctrl Monitor
								14	R	
BWENA	0	0	PE	CIC	EOIOE	SC	data	14	W	Bus Write Control
								15	R	
S8	0	S6	S5	S4	S3	S2	S1	15	W	Service Request Enable
								16	R	
EOS7-1	EOS6-1	EOS5-1	EOS4-1	EOS3-1	EOS2-1	EOS1-1	EOS0-1	16	W	EOS 1
							SRQS	17	R	Test register
EOS7-2	EOS6-2	EOS5-2	EOS4-2	EOS3-2	EOS2-2	EOS1-2	EOS0-2	17	W	EOS 2

6. Functional Characteristics

The iGPIP performs various functions in order to provide a high-performance microprocessor interface to the GPIB.

6.1.NEC µPD 7210 C Compatibility

Upon RESET, the iGPIB is in the NEC µPD 7210 C compatibility (*compatible mode*). This mode is active until the chip is swiched to the native mode (*extended mode*) via the *extended mode* auxiliary command. The *compatible mode* is provided for the compatibility with software written for the NEC µPD 7210 C. New software should always use the *extended mode*. Using *compatible mode*, only the functions also implemented in the NEC µPD 7210 C can be used. For all native functions the chip must be switched to *extended mode*.

If the 40-pin DIL version is used with a 8 MHz clock source (the original NEC µPD 7210 C uses a 1..8 MHz clock), the iGPIB provides a software and hardware compatible replacement for the NEC µPD 7210 C.

6.2.Data Transfer

Data transfer to or from the GPIB is performed via two 255 byte deep FIFO registers. These FIFOs are used to decouple GPIB traffic from the CPU bus.

If the GPIB is used to realize an IEEE488.2 *device*, the FIFO may be used as the *input* or *output queue*, respectively. This simplifies software design significantly. In addition, provisions are made to support the IEEE488.2 *trigger control* and to support the MAV status bit directly in hardware (a unique feature of the iGPIB).

The FIFOs are accessed by normal CPU read and write accesses to the Data In or Byte Out registers, respectively. Using the technique combined with repetitive move instructions (e. g. REP INSB of the 80386 CPU) provides the full 1 MByte/sec. transfer speed without using DMA.

6.3.Timeout

Usually, GPIB controller application software provides the user with a timeout feature, which aborts data tranfers without a functioning source or acceptor. The iGPIB provides a *timeout* interrupt condition. If this condition is unmasked, a timer counts down for a programmable interval. During normal operation, the timer is reset to its intial value whenever a data transfer takes place. If the handshake gets stuck, the timer underflows and an interrupt occurs.

6.4.Transfer Counter

The iGPIB has a 16 bit wide transfer counter. This counter reduces programming for DMA operations in two ways.

First, the counter delivers an end-of-transfer interrupt if a programmable amount of data has been sent respectively received. Driver software can initiate a DMA transfer and then switch to another task until the interrupt occurs.

Second, *a last byte handling* feature allows to automatically send the last byte with EOI true. On send transfers, it indicates the end of a data block. On receive transfers, it is possible to automatically signal RFD false after the last byte has been received. This enables the Controller to take control synchronously. With previous GPIB controllers like the NEC µPD 7210 C, all these operations had to be programmed explicity.

6.5.IEEE488.2 Service Request

In order to integrate the preferred implementation of requesting service, the iGPIB realizes the *Service-Request-Enable* register on chip. This allows to update the status byte via the status byte register independent of requesting service. Together with two *transition filters* for each status bit, the iGPIB handles the service request generation autonomously without any software intervention. Further, the MAV bit of the IEEE488.2 status byte can be reset automatically if a data block has been sent. This solves the problem of speed differences between device and controller which has not been dealt with by the IEEE488.2 standard.

6.6.Stop-Handshake Conditions

For Controllers, the IEEE488.2 standard particularly recommends to provide more than one stop-handshake condition. Previous controllers allow only EOI and one EOS bytes to be used for the stop-handshake condition. The

iGPIB allows EOI and up to three EOS byte to be used. The iGPIB entirely meets the standards recommendations in hardware that way reducing software overhead. In addition, the controller allows to *ignore* EOI as a stop-handshake condition. This simplifies the handling of pre-488.2 devices and devices not operating according to the standard.

6.7.BusLine Control and Monitoring

The iGPIB can independently control and monitor each bus line as well as the transceiver control signals. This exceeds the requirements of IEEE488.2 (monitoring of NRFD and NDAC).

6.8.Synchronous DMA Interface

The iGPIB FIFO may be accessed via the synchronous DMA interface (XDMA). This interface enables FIFO access without using the CPU data bus. XDMA can transfer data at a speed of up to 30 MByte/sec. This general interface may be used for various purposes. For example, high speed instruments may transfer data directly to the GPIB without any CPU intervention. Computers acting as GPIB controllers can perform DMA cycles utilizing the full band width of their busses, even with 64-bit architectures.

7. Function Description

7.1.Operating Modes

The chip can operate in *compatible mode* and in *extended mode*. The operating mode control is handled by the auxiliary command X_MODE.
In *compatible mode* the FIFO depth is set to 1. The controller state machine and the source handshake accord with the standard.
In *extended mode* the iGPIB has the following modified facilities:

- The source handshake acts according to IEEE488.2 standard modification. The NDAC line must be activated by an acceptor before a byte can be sent.
- Up to 3 bytes may be used for END recognition.
- The internal message "rsv" is generated according to IEEE488.2 chapter 11.
- The auxiliary command "rfd holdoff" generates a holdoff in ANRS state.
- A programmable 16-bit timer generates a maskable interrupt "tmo" whenever a time limit violation (time out) has occured during handshake.
- The SCAS state is available at the Pin SC (PLCC and TQFP only).
- All GPIB lines can be watched and controlled by the extension registers.
- A programmable 16-bit transfer counter is accessable. On talker transfer, an END message may be sent with the last byte transfered. On listener transfer, a RFD-holdoff may be performed. In both cases a maskable interrupt TC will be generated.
- For Data In and Byte Out registers a 255 byte FIFO can be enabled independently.
- The latency T1 can be set to 2000 ns, 1100 ns, 700 ns, 500 ns, 350 ns and 250 ns.
- A fast synchronous DMA-interface to the processor is available (PLCC and TQFP only).

7.1.1.Data Registers with FIFO

Data registers are the byte-out- and the data-in-register[5]. Both registers are implemented as FIFOs. In *compatible mode* the FIFOs are always 1 byte deep. In *extended mode* DI- and BO-FIFO can be individually switched from 1 to 255 byte depth. The registers input FIFO count and the output FIFO count indicate the number of bytes in their corresponding FIFO. They can only contain the values 0 or 1 when set to depth 1. Operating errors are indicated by the FIFO error interrupt (i. e. writing to full or reading from emty FIFO). Switching a FIFOs depth from 1 to 255 and vice versa clears it.

7.1.2.Interrupt Register

In both operating modes, 2 write registers, and 2 read registers for interrupt handling are available. They can be accessed at the addresses 1 and 2. Reading the interrupt state registers clears the corresponding interrupts. 13 interrupt conditions are indicated by the interrupt registers, each represented by 1 bit. All interrupts can be masked

[5]The term Data In register is used because only data bytes are received by this register while in controller idle state (CIDS). The term Byte Out shows that both data (CIDS) and commands (in controller active state) are sent through this register.

by writing to the interrupt mask register at the corresponding address. Any bit set in the interrupt mask register causes an interrupt, if a 1 occures in the corresponding interrupt status register. Via the auxiliary register bit B3 the interrupt output can be switched from active-high to active-low.

7.1.2.1.Register Table

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Adr.(HEX)	R/W	Name
CPT	APT	DET	END	DEC	ERR	DO	DI	1	R	Status 1
INT	SRQI	LOK	REM	CO	LOKC	REMC	ADSC	2	R	Status 2
CPT	APT	DET	END	DEC	ERR	DO	DI	1	W	Mask 1
0	SRQI	DMAO	DMAI	CO	LOKC	REMC	ADSC	2	W	Mask 2

7.1.2.2.Interrupt Bits in the Interrupt Status Register

1. CPT (Command Pass Through)
   This bit indicates that an undefined command has been received via GPIB or that a secondary command has been received following to an unknown command. It will only be set, if the auxiliary register bit B_0=1, which makes it possible to pass unknown commands to the processor. The handshake will be held off until the auxilary command "valid" is signaled by the CPU.
2. APT (Address Pass Through)
   This bit indicates that a secondary address has been received, which has to be checked by the CPU. This is only provided in address mode 3. The handshake will be held off until one of the auxiliary commands "valid" or "not valid" is issued by the CPU.
3. DET (Device Trigger)
   This bit indicates that a trigger message (GET when LADS) has been received.
4. END (END message received)
   This bit indicates that either the EOI or the EOS (data in register equals EOS register) message has been received.
5. DEC (Device Clear)
   This bit indicates that a clear (DCL or SDC when LADS) message has been received.
6. ERR (Error)
   This bit indicates that the contents of the Byte Out register has been lost. It will be set if data has been sent without listener addressed or if a byte has been written to the Data Out register during source idle state (SIDS).
7. DO (Data Out)
   This bit indicates a data write request to the Byte Out register. The bit is set, if the FIFO has been full (i.e. 1 or 255 bytes) and the FIFO is not full anymore (i.e. <1 or <255 bytes).
8. DI (Data In)
   This bit indicates a reception of a data byte from the GPIB Bus. The bit is set if the FIFO has been empty and is not empty anymore. In continuous mode it will never be set.
9. SRQI (Service Request Input)
   This bit indicates that a service request (SRQ) has been received. A SRQ message can only be received if the chip is controller in charge (CIC bit in the address mode register set).
10. LOKC (Lockout Change)
    This bit indicates that the LOK-bit in interrupt status register 2 has changed.
11. REMC (Remote Change)
    This bit indicates that the REM-bit in interrupt status register 2 has changed.
12. ADSC (Address Status Change)
    This bit indicates that one of the bits TA, LA, CIC or MJMN has changed in the address status register.
13. CO (Command Output)
    This bit is set in controller active state whenever an interface message can be written to the Byte Out register.

7.1.2.3.Non Interrupt Bits in the Interrupt State Register

- LOK, REM (Lockout, Remote)
  These bits indicate the state of the remote/lockout function. The LOK-bit indicates if the function is in local or remote with lockout state (LWLS or RWLS). The REM-bit indicates that the function is in remote state (REMS) or remote with lockout state (RWLS).

- DMAO, DMAI (DMA Output, DMA Input)
  These bits are controlling the DMA-transfer between memory and GPIB bus. If DMAO=1 and the byte-out FIFO is not full, a DMA-request will be generated. If DMAI=1, a DMA-request will be generated as soon as a byte has been received from the GPIB bus.

- INT (Interrupt)
  This bit indicates that an interrupt has occured. It is generated by an OR operation of all unmasked interrupt bits.

7.1.3.Serial Poll Register

The serial poll register can be read or written on address 3. The CPU writes the status byte (STB) into this register, which shall be sent when a controller performs a serial poll. If the CPU sets the "rsv" bit to 1, the internal message "rsv" will be initialed. This generates a service request (SRQ line set) as soon as the chip is not in SPAS state. The rsv-bit is cleared during serial poll to reset the SRQ line.
The CPU can read the status byte (STB), written to the serial poll mode register, from the serial poll status register. Testing the PEND-bit checks if the serial poll request has been satisfied: the PEND-bit is set when the rsv-bit becomes 1. It is cleared when the serial poll function changes from APRS to NPRS. This way it can be checked if the the GPIB controller has already satisfied the service request.
In *extended mode* the chip provides a service request enable register which allows automatic service request generation when a bit in the status byte is set. If a bit is set from 0 to 1 and the corresponding mask bit in the service request enable register is set, a service request is autmatically generated by the chip. The rsv-bit of the SRQ status register is meaningless in *extended mode*, because the SRQ is generated automatically.
If the MAVEN-bit is set in *extended mode*, the SRQ status register bit 4 (MAV: message available; IEEE488.2 standard) is automatically cleared if a byte has been sent with EOI.

7.1.3.1.Register Table

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Adr.(HEX)	R/W	Name
S8	rsv	S6	S5	S4	S3	S2	S1	3	W	Mode
S8	PEND	S6	S5	S4	S3	S2	S1	3	R	Status
S8_EN	x	S6_EN	S5_EN	S4_EN	S3_EN	S2_EN	S1_EN	15	W	Service Request Enable

7.1.4.Address Mode & Status Register

The address mode register is used to specify the signals at T/R2 and T/R3. It is also used to set address mode. The states of various interface functions can be inquired from the address status register.

7.1.4.1.Register Table

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Adr.(HEX)	R/W	Name
ton	lon	TRM1	TRM0	IFENA	OFENA	ADM1	ADM0	4	W	Address Mode
CIC	ATN~	SPMS	LPAS	TPAS	LA	TA	MJMN	4	R	Address Status

The bits TRM0 and TRM1 are evaluated by the GPIB interface and define the function of the pins T/R2 and T/R3:

TRM1	TRM0	T/R2	T/R3
0	0	EOIOE: End or Identify Output Enable	TRIG: Trigger
0	1	CIC: Controller in Charge	TRIG: Trigger
1	0	CIC: Controller in Charge	EOIOE: End or Identify Output Enable
1	1	CIC: Controller in Charge	PE: Parallel Poll Enable

The bits ton, lon ADM0 and ADM1 specify the address mode:

ton	lon	ADM1	ADM0	Address Mode	contents of addr. reg. 0	contents of addr. reg. 1
1	0	0	0	talk only	not used	not used
0	1	0	0	listen only	not used	not used
0	0	0	1	Address Mode 1	first primary talker-(listener-) address	second primary talker-(listener-) address
0	0	1	0	Address Mode 2	first primary talker-(listener-) address	second primary talker-(listener-) address
0	0	1	1	Address Mode 3	first primary talker-(listener-) address	second primary talker-(listener-) address

- Talk only or Listen only (ton or lon = 1):
  In this mode, the recognition of the device address is not needed. Therefore, the address registers are not used.

- Address-Mode 1:
  In this mode, only primary addresses are used for talker and listener addressing. Up to 2 device addresses will be recognized.

- Address-Mode 2:
  Talker/listener are operating in *extended mode* (TE, LE). Primary and secondary addresses are required to perform addressing. The recognition of primary and secondary address is managed by the hardware. A second device address will not be recognized.

- Address-Mode 3:
  Talker/listener are operating in *extended mode* (TE, LE). Primary and secondary addresses are required to perform addressing. The identification of the secondary address must be done by the CPU. Two primary device addresses may be recognized.

The bits IFENA and OFENA makes it possible to set input and output FIFO seperately to the size of 255 bytes.

The bits ATN~, LPAS, TPAS, CIC, LA, TA, MJMN and SPMS indicate the states of the interface functions. The bit ATN~ indicates that the controller function has entered standby state. LPAS and TPAS indicate the listener/talker primary addressed state.
Changes of the bits CIC, LA, TA and MJMN initiate an ADSC interrupt.
The bit SPMS (Serial Poll Mode State) indicates whether a serial poll is in progress. It is set with SPE and it is cleared by SPD or IFC.

7.1.5.Address Registers

There are 2 address read registers and 1 address write register. Depending on the ARS-bit the write register can access two 7-bit wide registers. These registers contain a 5-bit wide address and the infomation whether this address represents a talker, a listener or both.
The bit ARS (Address Register Select) specifies into which of the address registers the bits 0-6 shall be written:
ARS = 0 → selects address register 0. The specified address (AD1-AD5) will be recognized as talker address, if bit DT (Disable Talker) = 0. Bit DL (Disable Listener) = 0 specifies the address as a listener address. The bits DL0, DT0, DL1 and DT1 in the read registers correspond to the DL and DT bits in the write register. The bit EOI indicates the state of the EOI line when the data byte found in the data-in register has been received.
As system controller the bit T8run can be used to check if 100 µs have expired since setting of the IFC- or resetting of the REN-line. A value of 1 indicates that the standard latency has not yet been reached.

7.1.5.1.Register Table

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Adr.(HEX)	R/W	Name
ARS	DT	DL	AD5	AD4	AD3	AD2	AD1	6	W	Register 0/1
T8run	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0	6	R	Register 0
EOI	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1	7	R	Register 1

7.1.6.Command Pass Through Register

In controller idle state the CPT-register can be used to determine the state of the data lines of the GPIB. It is necessary if a DAC holdoff has been initiated and the CPU must qualify the actual interface message.
In controller active state the CPT-register stores the response of a parallel poll until interface messages will be sent on the GPIB again.

7.1.6.1.Register Table

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Adr.(HEX)	R/W	Name
CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0	5	R	CPT-Register

7.1.7.EOS Register

This register contains the 7- or 8 bit wide END message which is used to detect the end of a data block transfer. The EOS width will be specified by the auxiliary register bit A4 (eos-width). The END signal is determined in the system EOS register by comparing the GPIB data word and the EOS register. In *extended mode* there are 2 additional registers. Their contents can be used for END message detection too. A 7-bit wide END message detection can only be performed by with the compatible EOS register. The additional registers can be masked, by using the extension register bits END_ENA1 and END_ENA2 for end message detection.

7.1.7.1.Register Table

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Adr. (HEX)	R/W	Name
EOS7	EOS6	EOS5	EOS4	EOS3	EOS2	EOS1	EOS0	7	W	EOS Register 0
E1-7	E1-6	E1-5	E1-4	E1-3	E1-2	E1-1	E1-0	16	W	EOS Register 1
E2-7	E2-6	E2-5	E2-4	E2-3	E2-2	E2-1	E2-0	17	W	EOS Register 2

7.1.8.Auxiliary Registers

The auxiliary register system consists of 4 auxiliary registers and 2 command registers. The auxiliary registers contain information like the holdoff mode and the END message handling.

7.1.8.1.Register Table

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Adr. (HEX)	R/W	Name
CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0	5	W	Auxiliary Register

A write access to this register can initiate one of the following operations:

a. Write access to auxiliary register A, B or E
b. Write access to the parallel poll register
c. A write to the clock frequency register is ignored
d. Execution of an auxiliary command.
There are two additional operations available in *extended mode*:
e. Execution of an extended auxiliary command
f. Write access to auxiliary register D.

CNT			COM					Operation
2	1	0	4	3	2	1	0	
0	0	0	C_4	C_3	C_2	C_1	C_0	Auxiliary command execution
0	0	1	0	0	0	0	0	reserved
0	1	0	D_4	D_3	D_2	D_1	D_0	Auxiliary register D
0	1	1	U	S	P_3	P_2	P_1	Parallel poll register
1	0	0	A_4	A_3	A_2	A_1	A_0	Auxiliary register A
1	0	1	B_4	B_3	B_2	B_1	B_0	Auxiliary register B
1	1	0	0	E_3	E_2	E_1	E_0	Auxiliary register E
1	1	1	C_4	C_3	C_2	C_1	C_0	Ext. auxiliary command execution

7.1.8.2.Auxiliary Commands

Auxiliary commands are initiated by writing the byte $000C_4C_3C_2C_1C_0$ from the CPU into the auxiliary register. 21 commands are recognized in *compatible mode*. They can be used to signal internal messages and to specify various operating modes.

The new auxiliary command X_MODE switches the chip to *extended mode*. Switching back to µPD 7210 *compatible mode* can only be done by an external reset or by the auxiliary command CHIP RESET.

1. Immediate Execute pon	00000	This command inverts the state of the internal message POWER ON (pon). If pon=1 all interface functions become idle.
2. Chip Reset	00010	The command CHIP RESET performs the same function as an external reset and initiates the following: a. pon will be set b. All registers will be cleared. Exceptions: The extension register burstlength will be set to 1. The external reset is linked to the software reset in this system.
3.Finish Handshake	00011	This command ends handshake by releasing the RFD holdoff state.
4. Trigger	00100	The command generates a trigger pulse at pin T/R3, if this signal is enabled at the pin. This causes the same reaction as the active state of the trigger function and will be combined with that state.
5.Return to Local	0X101	This command generates the internal message RTL. If X=1, then RTL will be set, otherwise RTL will be reset or respectively pulsed.
6. Send EOI	00110	The next data byte will be sent with the END message. This can only be done in TACS. The evaluation is performed in the byte out FIFO.
7. Not Valid	00111	A handshake which has been held off by "address pass through", will continue. The secondary address has been qualified as "not valid" by the CPU.
8. Valid	01111	A handshake which has been held off by "address pass through", will continue. The secondary address has been qualified as "valid" by the CPU.
9.Set Parallel Poll Flag	0X001	This command sets the parallel poll flag to the value of bit C_3(=X). If the auxiliary register bit B_4=0, the value of this flag will be handled as internal message "ist" (individual status). Otherwise the service request state (SRQS) will be used as "ist" signal.
10. Go to Standby	10000	This command generates the internal message "gts". The message will be cleared when the controller has left the active state (CACS).
11. Take Control Async	10001	This command pulses the internal message "tca".
12. Take Control Synchronously	10010	This command sets the internal message "tcs". The message will be cleared when the controller has switched to active state (CACS).
13. Take Control Synchronously on End	11010	This command sets the internal message "tcs" as soon as an END message (refer to Interrupt Registers) has been generated in controller standby state (CSBS). "tcs" is cleared when the controller has switched to active state (CACS).
14. Listen	10011	This command pulses the internal message "ltn". If necessary, the continuous mode will be disabled.
15. Listen in Continuous Mode	11011	This command pulses the internal message "ltn". In addition, the continuous mode will be enabled. This mode will be disabled when the auxiliary command "ltn" is detected or LIDS (listener idle state) is entered..
16. Local Unlisten	11100	This command pulses the internal message "lun" with the duration of 1 clock pulse.
17. Execute Parallel Poll	11101	This command generates the internal message "rpp". The message will be cleared when the controller enters the idle state (CIDS) or parallel poll state (CPPS).
18. Set/Clear IFC	1X110	This command generates the internal message "rsc" and sets "sic" to the value of bit 3(=X).
19. Set/Clear REN	1X111	This command generates the internal message "rsc" and sets "sre" to the value of bit 3(=X).
20. Disable System Control	10100	This command clears the internal message request system control (rsc).
21. Extended Mode	01010	The chip switches to extended mode.
22. Go TMS9914A	11000	The chip switches to TMS9914A mode. Chip reset is issued. Usable in chips with QFP80 package only.

The following auxiliary commands are available in *extended mode*. The CPU can write to the auxiliary register using the byte $111C_4C_3C_2C_1C_0$.

1. Disable Listener	00000	Disables the listener function.
2. Enable Listener	00001	Enables the listener function.
3. map_1	00010	Maps register bank 1 to the addresses of register bank 0 for following read/write access.
4. map_2	00011	Maps register bank 2 to the addresses of register bank 0 for following read/write access.
5. not_ready	00100	Initiates a RDF-holdoff.
6. out FIFO clear	00101	Clears BO-FIFO counter.
7. in FIFO clear	00110	Clears DI-FIFO counter.

7.1.8.3.Clock Frequency Specification F

Not used by the current type.

7.1.8.4.Parallel Poll Register

Writing the byte $011USP_3P_2P_1$ to the auxiliary register allows to write to the parallel poll register. When using the subset PP1 (remote configuration) it should not be written to this register. In this case the PPE message issued by the controller defines the parallel poll message. A PPD message issued by the controller disables the parallel poll response.

When using subset PP2 (local configuration) the response message must be written to this register in advance. The parallel poll response line is specified by the first 3 bits of this register. The 4th bit specifies, if the chosen line will be set true or false on occurence of the internal message "ist" (individual status): The message will be set true if "ist" equals bit S (4th bit). The 5th bit U contains the internal message "lpe~". If U = 0, the response to the parallel poll response is enabled. If U = 1, the parallel poll response is disabled and the bits S and P_{1-3} have no meaning, they should be reset to 0.

7.1.8.5.Auxiliary Register A

The 5 bits of the auxiliary register A are used to specify handshake mode and the EOS message handling. The bits A_0 and A_1 specify the handshake mode. The bits A_2, A_3 and A_4 specify the EOS handling:

A1	A0	Handshake Mode
0	0	normal
0	1	Blocked RFD message for all data
1	0	Blocked RFD message for END message
1	1	Continuous mode

A_2	=1 → END interrupt bit set when EOS received
A_3	=1 → EOI set on EOS sent
A_4	=1 → EOS 8-bit wide, =0 → EOS 7-bit wide

7.1.8.6.Auxiliary Register B

The auxiliary register B specifies special hardware features of the chip.

B_0	If b_0 is set, the interrupt bit CPT will become true on the detection of an unknown command.
B_1	If b_1 is set, the EOI line will be set together with the status bit in SPAS.
B_2	High speed mode: If set T1 is reduced to 500 ns.
B_3	Defines the active level of the interrupt signal INT. B_3=0 → active high
B_4	Specifies the source of internal message "ist": B_4=0 → ist = parallel poll flag B_4=1 → ist = SRQS (service request state)

7.1.8.7.Auxiliary Register D

The auxiliary register D is available in *extended mode*. It specifies the latencies T1 and T6 described in IEEE488 standard. D_4 = 1 increases time T6 from 2 µs to 50 µs. This allows parallel polling on systems with slow bus extenders. D_0-D_3 specify T1 for high speed and normal mode according to the following table:

D_3	D_2	D_1	D_0	First byte sent after ATN_false	Following bytes in fast mode
0	0	x	x	2000 ns	x
0	1	x	x	1100 ns	x
1	0	x	x	700 ns	x
x	x	0	0	x	500 ns
x	x	0	1	x	350 ns
x	x	1	0	x	250 ns

7.1.8.8.Auxiliary Register E

The auxiliary register E consists of 2 bits in *compatible mode*. They specify the DAC holdoff handling. If E_0 = 1 the handshake is held off on a clear command issued by the GPIB controller (detectable by DCSA). If E_1 = 1 the handshake is held off when the GPIB controller issues a trigger command (detecable by DTAS).
In *extended mode* the auxiliary register E keeps 2 additional bits. If E_2 = 1, any command received will be initate a DAC holdoff (bit cmd is set in the extended interrupt register). In the same way the reception of TCT command will initiate a DAC holdhoff if E_3 = 1.
The DAC holdoff is cleared by the auxiliary commands "valid" or "not valid". This enables the handshake to continue. The command TCT is executed only if the holdoff has been terminated by the auxiliary command "valid". Otherwise this command is ignored.

Bit	Holdoff with command(s)	Meaning
E_0	DCL, SDC	Device Clear
E_1	GET	Trigger
E_2	all	
E_3	TCT	Take Control

7.1.9.Transfer Counter

The programmable 16-bit transfer counter counts bytes sent/received via the GPIB bus if it participates as talker/listener.
The requested number of bytes must be stored in the counter. Every byte transferred via GPIB decrements the counter by 1, if the bit TC_ENA is set in the extended mode register. When the counter reaches 0 the maskable interrupt TC is issued and the counter stops. If the TC_LBH bit is set, the EOI line is set with the last byte on writing (TC_TLK must be 1) and after reading (TC_TLK must be 0) the last byte a RDF holdoff is started (all bits in the exetended mode register at Address Hex F). The counter is readable too.

7.1.9.1.Register Table

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Adr. (HEX)	R/W	Name
TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0	B	W/R	TC lower byte
TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8	C	W/R	TC upper byte

7.1.10.Timeout Register

In *extended mode* a timeout timer registers the violation of a maximum latency per byte at handshake, generating the maskable interrupt "tmo".
The 16-bit timer is programmable by 2 registers. The 16-bit value composed of both registers represents the maximum latency in milliseconds. The backward counter restarts always with the programmed count whenever no byte has been received on listener transfer or no byte has been fetched on talker transfer.

7.1.10.1.Register Table

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Adr. (HEX)	R/W	Name
TO7	TO6	TO5	TO4	TO3	TO2	TO1	TO0	D	W	TO lower byte
TO15	TO14	TO13	TO12	TO11	TO10	TO9	TO8	E	W	TO upper byte

7.1.11.Watermark Register / FIFO Counter Register

The threshold which generates the extended interrupts IF_WM/OF_WM is specified in both watermark registers. The current filling level of the DI FIFO and the free space of the BO FIFO respectively are compared with the corresponding watermark register. When the filling level of the DI-FIFO is higher or equal to the specified value the signal IF_WM is true. In addition,OF_WM is true if the free space in the BO-FIFO is higher or equal to the specified value. Using the count register,the current filling levels of both FIFOs can be inquired directly.

7.1.11.1.Register Table

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Adr. (HEX)	R/W	Name
IFC7	IFC6	IFC5	IFC4	IFC3	IFC2	IFC1	IFC0	10	R	Input FIFO Count
IFW7	IFW6	IFW5	IFW4	IFW3	IFW2	IFW1	IFW0	10	W	Input FIFO Watermark
OFC7	OFC6	OFC5	OFC4	OFC3	OFC2	OFC1	OFC0	11	R	Output FIFO Count
OFW7	OFW6	OFW5	OFW4	OFW3	OFW2	OFW1	OFW0	11	W	Output FIFO Watermark

7.1.12.Extended Interrupt Registers

In *extended mode* there are 15 additional interrupt conditions available. According to the compatible interrupts they can be polled by 2 status registers and are maskable by 2 mask registers. A read access clears the interrupt status register. To create the interrupt signal the extended interrupts are combined with the compatible interrupt registers.

7.1.12.1.Register Table

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Adr. (HEX)	R/W	Name
OF_WM~	IF_WM~	OFRDY	IFRDY	OF_EM	IF_FL	OF_WM	IF_WM	8	R	FIFO Status Register
	FF_ERR	ATN	IFC	TCT	CMD	TC	TMO	9	R	Interrupt Status 3
	FF_ERR	ATN	IFC	TCT	CMD	TC	TMO	9	W	Interrupt Mask 3
OF_WM~	IF_WM~	OFRDY	IFRDY	OF_EM	IF_FL	OF_WM	IF_WM	A	R	Interrupt Status 4
OF_WM~	IF_WM~	OFRDY	IFRDY	OF_EM	IF_FL	OF_WM	IF_WM	A	W	Interrupt Mask 4

7.1.12.2.Interruptbits

1. TMO (time out)
   Indicates elapsed timeout counter.
2. TC (transfer counter)
   Indicates that the transfer counter has counted down to 0.
3. CMD (command received)
   Indicates the reception of a GPIB command.
4. TCT (take control command received)
   Indicates the reception of the GPIB command TCT.
5. IFC (interface clear active)
   Indicates that the IFC line has become active.
6. ATN (attention active)
   Indicates that the ATN line has become active.

7. FF_ERR (FIFO error occured)
   Indicates that a FIFO operation error has occured (i.e. read from an empty FIFO or write to full FIFO).
8. IF_WM (input FIFO watermark reached)
   Signals a DI-FIFO threshold has been reached.
9. OF_WM (output FIFO watermark reached)
   Signals a BO-FIFO threshold has been reached.
10. IF_FL (input FIFO full)
    Indicates DI-FIFO full.
11. OF_EM (output FIFO empty)
    Indicates BO-FIFO empty.
12. IFRDY (input FIFO ready)
    Indicates that the DI-FIFO contains at least 1 byte.
13. OFRDY (output FIFO ready)
    Indicates that the BO-FIFO has free space for at least 1 byte.
14. IF_WM~ (has left input FIFO watermark)
    Indicates a DI-FIFO watermark underflow.
15. OF_WM~ (has left output FIFO watermark)
    Indicates a BO-FIFO watermark underflow.

7.1.13.Miscellaneous Extension Registers

The revision code register, the OEM code register, the extended status register, the extended mode register, and the XDMA control register are combined in this section.
The version number of the chip is stored in the revision code register. The OEM code register contains the identification of a probable special design.
If the EOIDIS bit in the *extended mode* register is set, the chip does not notify EOI as the end of an interrupt generation respectively at holdoff on end. The TRGEN bit makes it possible to generate a trigger pulse at pin T/R3.
OF_FL indicates that the BO-FIFO is full and IF_EM indicates that the DI-FIFO is empty.
The LIDS bit indicates that the listener function has been disabled by the corresponding auxiliary command. The SCSEL bit indicates the state of the SCSEL pin (PLCC and TQFP only). The OQMU bit (output queue message unit in progress) indicates a string transfer in progress. This bit is set when a byte is sent and is reset when a byte has been sent with EOI.

The DMAX and DMA_O bits in the XDMA control register are controlling the synchronous DMA interface:
XDMA enables the synchronous DMA mode.
DMA_O specifies the transfer direction: high means DMA output (GPIB Talker); low means DMA input (GPIB Listener).
The DMA_S specifies if the FIFOs will be accessed every cycle (=high) or only every second cyle (=low).
The AUX_O bit defines the width of the synchronous DMA transfer: high stands for 16 bit, low means 8 bit.
The bit is only passed to the pin, because the conversion from 8- to 16-bit performed externally.

7.1.13.1.Register Table

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Adr. (HEX)	R/W	Name
REVC7	REVC6	REVC5	REVC4	REVC3	REVC2	REVC1	REVC0	D	R	Revision Code Register
OEM7	OEM6	OEM5	OEM4	OEM3	OEM2	OEM1	OEM0	E	R	OEM Code Register
			OF_FL	IF_EM	LIDIS	SCSEL	OQMU	F	R	Extended Status
TC_LBH	TC_TLK	TC_ENA	EOIDIS	E2ENA	E1ENA	MAVEN	TRGEN	F	W	Extended Mode
				AUX_O	DMA_S	DMAX	DMA_O	8	W	XDMA Control Register

7.1.14.GPIB Monitor Registers

The monitor registers enable the CPU to read and write the GPIB lines avoiding the chip logic.
Via read access to the bus data monitor register (BDM) and the bus control monitor register (BCM) the current status of the GPIB lines can be obtained without combination with chip internals. If the BW_ENA bit is set, the contents of the write registers BDM and BCM will be directly connected to the GPIB. The values BWDir_DATA,

BWDir_PE, BWDir_SC, BWDir_EOIOE and BWDir_CIC specify the data direction of the pads and the value at the output pads T/R1, T/R2, T/R3, SC and CIC: If BWDir_DATA is set, DIO1..8 are outputs, NRFD and NDAC are inputs and vice versa. If BWDir_SC is set, REN and IFC are outputs. If BWDir_EOIOE is set, EOI is an output. If BWDir_CIC is set, SRQ is an input. BWDir_PE affects only T/R3. If defined as PE, the contents of this bit applies to the pin.

7.1.14.1.Register Table

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Adr. (HEX)	R/W	Name
BDM7	BDM6	BDM5	BDM4	BDM3	BDM2	BDM1	BDM0	12	W/R	Bus Data Monitor
EOI	REN	SRQ	ATN	IFC	NDAC	NRFD	DAV	13	W/R	Bus Control Monitor
BW_ENA			PE	CIC	EOIOE	SC	Data	14	W	Bus Write Direction

7.1.15.Test Register

This register contains information about the service request state. The other bits are undefined and may change in following releases.

7.1.15.1.Register Table

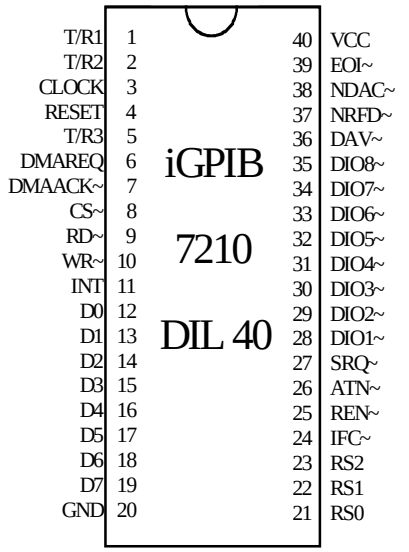
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Adr. (HEX)	R/W	Name
							SRQS	16	R	Test Register

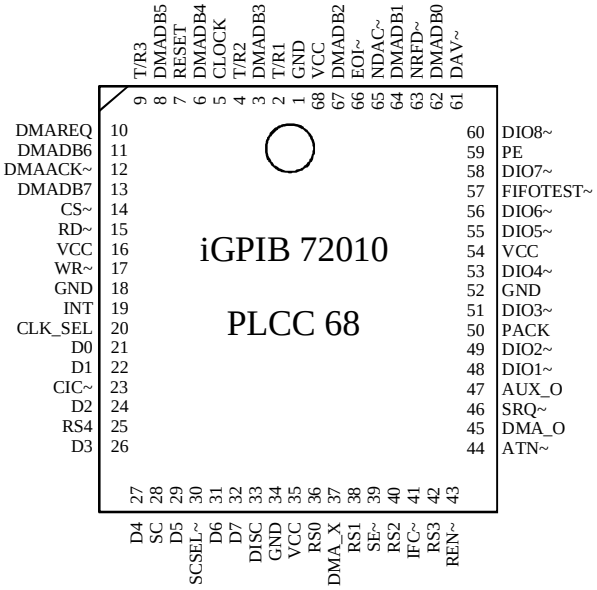
7.1.16.GPIB Command Decoder

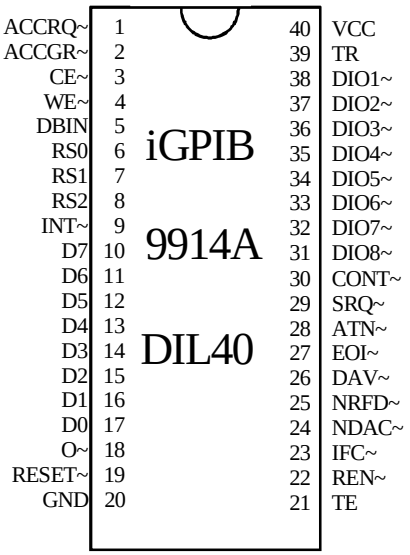
The command decoder recognizes interface commands sent via the GPIB. Interface commands are transferred with ATN active on the data bus. The decoder transforms the ATN signal as well as the data byte of the GPIB into signals that indicate interface messages.

Interface Message	Byte	ATN	Generated Signal	Meaning
UCG	X001XXXX	1	UCG	Universal Command Group
DCL	X0010100	1	DCL	Device Clear
LLO	X0010001	1	LLO	Local Lockout
PPU	X0010101	1	PPU	Parallel Poll Unconfigure
SPD	X0011001	1	SPD	Serial Poll Disable
SPE	X0011000	1	SPE	Serial Poll Enable
ACG	X000XXXX	1	ACG	Addressed Command Group
GET	X0001000	1	GET	Group Execute Trigger
GTL	X0000001	1	GTL	Go To Local
PPC	X0000101	1	PPC	Parallel Poll Configure
SDC	X0000100	1	SDC	Seclect Device Clear
TCT	X0001001	1	TCT	Take Control
LAG	X01XXXXX	1	LAG	Listener Address Group
TAG	X10XXXXX	1	TAG	Talker Address Group
UNL	X0111111	1	UNL	Unlisten
SCG	X11XXXXX	1	SCG	Secondary Command Group
PPE	X110SPPP	1	PPE	Parallel Poll Enable
PPD	X111XXXX	1	PPD	Parallel Poll Disable
RQS	X1XXXXXX	0	RQS	Request Service
PCG	ACG + UCG + LAG + TAG	1	PCG	Primary Command Group

8. Pinnings


T/R1 1
T/R2 2
CLOCK 3
RESET 4
T/R3 5
DMAREQ 6
DMAACK~ 7
CS~ 8
RD~ 9
WR~ 10
INT 11
D0 12
D1 13
D2 14
D3 15
D4 16
D5 17
D6 18
D7 19
GND 20
40 VCC
39 EOI~
38 NDAC~
37 NRFD~
36 DAV~
35 DIO8~
34 DIO7~
33 DIO6~
32 DIO5~
31 DIO4~
30 DIO3~
29 DIO2~
28 DIO1~
27 SRQ~
26 ATN~
25 REN~
24 IFC~
23 RS2
22 RS1
21 RS0
iGPIB
7210
DIL 40


T/R3 9
DMADB5 8
RESET 7
DMADB4 6
CLOCK 5
T/R2 4
DMADB3 3
T/R1 2
GND 1
VCC 68
DMADB2 67
EOI~ 66
NDAC~ 65
DMADB1 64
NRFD~ 63
DMADB0 62
DAV~ 61
DMAREQ 10
DMADB6 11
DMAACK~ 12
DMADB7 13
CS~ 14
RD~ 15
VCC 16
WR~ 17
GND 18
INT 19
CLK_SEL 20
D0 21
D1 22
CIC~ 23
D2 24
RS4 25
D3 26
60 DIO8~
59 PE
58 DIO7~
57 FIFOTEST~
56 DIO6~
55 DIO5~
54 VCC
53 DIO4~
52 GND
51 DIO3~
50 PACK
49 DIO2~
48 DIO1~
47 AUX_O
46 SRQ~
45 DMA_O
44 ATN~
D4 27
SC 28
D5 29
SCSEL~ 30
D6 31
D7 32
DISC 33
GND 34
VCC 35
RS0 36
DMA_X 37
RS1 38
SE~ 39
RS2 40
IFC~ 41
RS3 42
REN~ 43
iGPIB 72010
PLCC 68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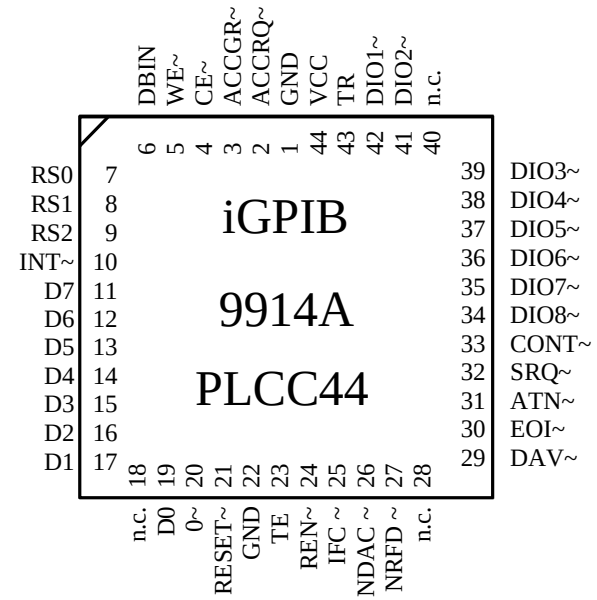
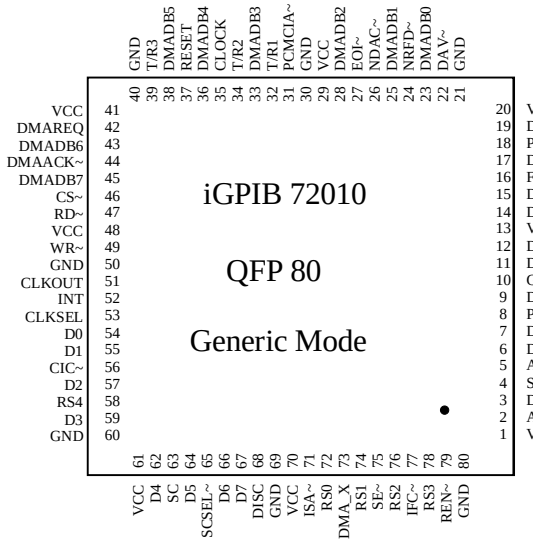
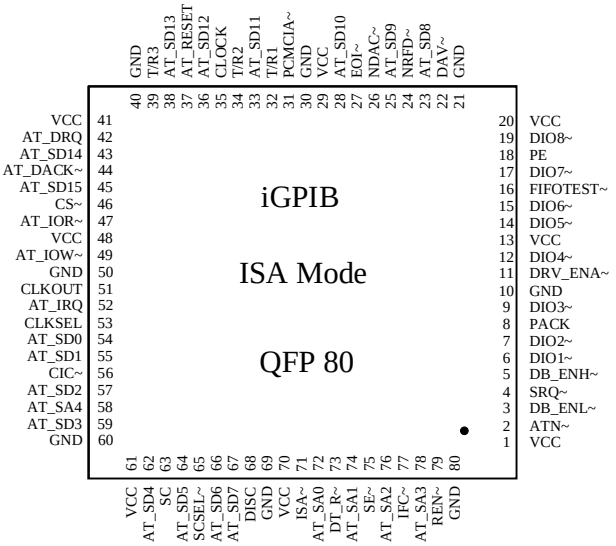
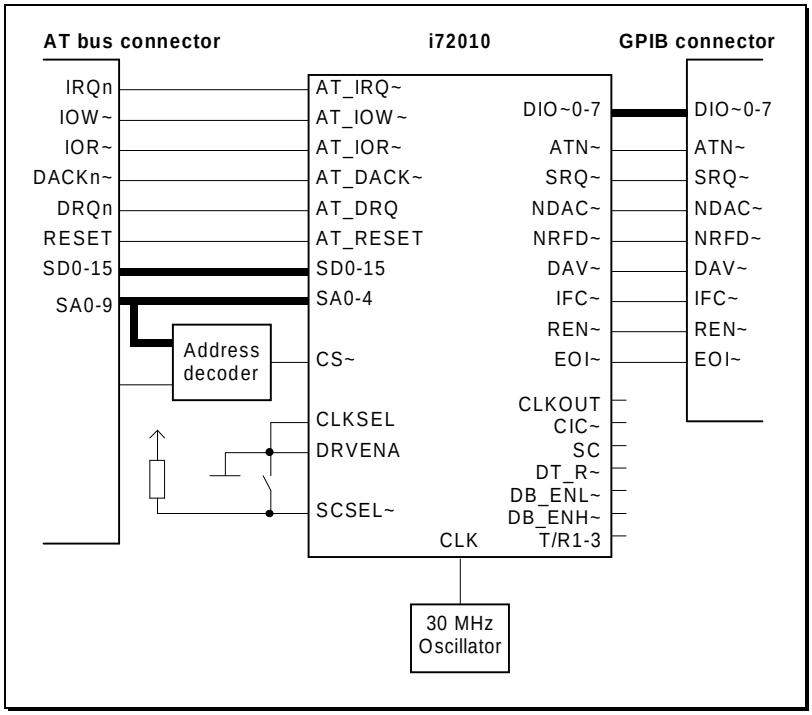
ACCGR~ 2
CE~ 3
WE~ 4
DBIN 5
RS0 6
RS1 7
RS2 8
INT~ 9
D7 10
D6 11
D5 12
D4 13
D3 14
D2 15
D1 16
D0 17
O~ 18
RESET~ 19
GND 20
40 VCC
39 TR
38 DIO1~
37 DIO2~
36 DIO3~
35 DIO4~
34 DIO5~
33 DIO6~
32 DIO7~
31 DIO8~
30 CONT~
29 SRQ~
28 ATN~
27 EOI~
26 DAV~
25 NRFD~
24 NDAC~
23 IFC~
22 REN~
21 TE
iGPIB
9914A
DIL40

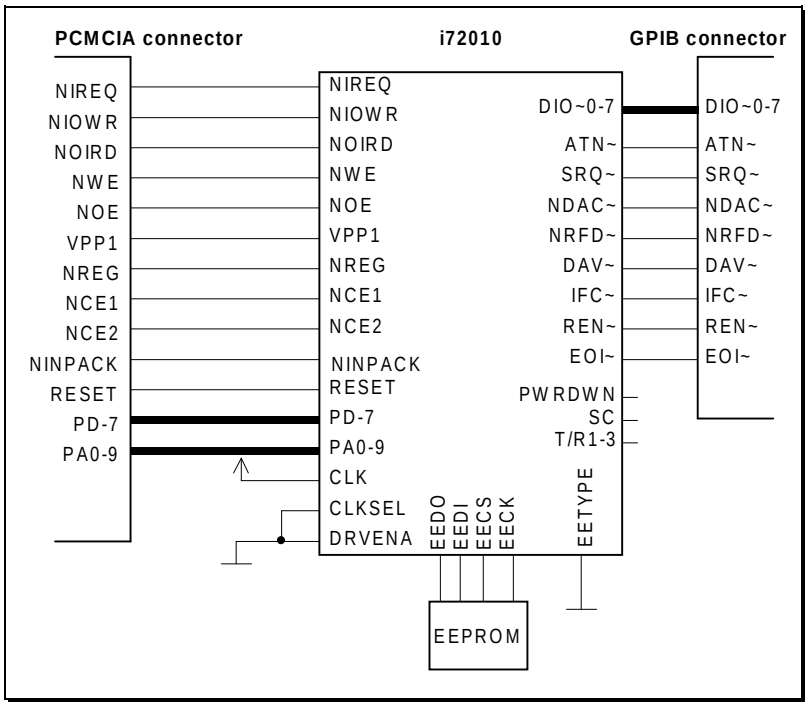

DBIN 6
WE~ 5
CE~ 4
ACCGR~ 3
ACCRQ~ 2
GND 1
VCC 44
TR 43
DIO1~ 42
DIO2~ 41
n.c. 40
RS0 7
RS1 8
RS2 9
INT~ 10
D7 11
D6 12
D5 13
D4 14
D3 15
D2 16
D1 17
39 DIO3~
38 DIO4~
37 DIO5~
36 DIO6~
35 DIO7~
34 DIO8~
33 CONT~
32 SRQ~
31 ATN~
30 EOI~
29 DAV~
n.c. 18
D0 19
0~ 20
RESET~ 21
GND 22
TE 23
REN~ 24
IFC ~ 25
NDAC ~ 26
NRFD ~ 27
n.c. 28
iGPIB
9914A
PLCC44


iGPIB 72010
QFP 80
Generic Mode
VCC 41
DMAREQ 42
DMADB6 43
DMAACK~ 44
DMADB7 45
CS~ 46
RD~ 47
VCC 48
WR~ 49
GND 50
CLKOUT 51
INT 52
CLKSEL 53
D0 54
D1 55
CIC~ 56
D2 57
RS4 58
D3 59
GND 60
61 VCC
62 D4
63 SC
64 D5
65 SCSEL~
66 D6
67 D7
68 DISC
69 GND
70 VCC
71 ISA~
72 RS0
73 DMA_X
74 RS1
75 SE~
76 RS2
77 IFC~
78 RS3
79 REN~
80 GND
40 GND
39 T/R3
38 DMADB5
37 RESET
36 DMADB4
35 CLOCK
34 T/R2
33 DMADB3
32 T/R1
31 PCMCIA~
30 GND
29 VCC
28 DMADB2
27 EOI~
26 NDAC~
25 DMADB1
24 NRFD~
23 DMADB0
22 DAV~
21 GND
20 VCC
19 DIO8~
18 PE
17 DIO7~
16 FIFOTEST~
15 DIO6~
14 DIO5~
13 VCC
12 DIO4~
11 DRV_ENA~
10 GND
9 DIO3~
8 PACK
7 DIO2~
6 DIO1~
5 AUX_O
4 SRQ~
3 DMA_O
2 ATN~
1 VCC

iGPIB 72010
QFP 80
PCMCIA Mode
VCC 41
NINPACK 42
NWE~ 43
VPP1 44
EEDO 45
NCE1~ 46
NIORD~ 47
VCC 48
NIOWR~ 49
GND 50
PWRDWN 51
NIREQ~ 52
CLKSEL 53
PD0 54
PD1 55
NOE~ 56
PD2 57
PA4 58
PD3 59
GND 60
61 VCC
62 PD4
63 SC
64 PD5
65 NREG~
66 PD6
67 PD7
68 DISC
69 GND
70 VCC
71 ISA~
72 PA0
73 EEDI
74 PA1
75 SE~
76 PA2
77 IFC ~
78 PA3
79 REN~
80 GND
40 GND
39 T/R3
38 NCE2~
37 RESET
36 PA9
35 CLOCK
34 T/R2
33 PA8
32 T/R1
31 PCMCIA~
30 GND
29 VCC
28 PA7
27 EOI~
26 NDAC~
25 PA6
24 NRFD~
23 PA5
22 DAV~
21 GND
20 VCC
19 DIO8~
18 PE
17 DIO7~
16 FIFOTEST~
15 DIO6~
14 DIO5~
13 VCC
12 DIO4~
11 DRV_ENA~
10 GND
9 DIO3~
8 PACK
7 DIO2~
6 DIO1~
5 EECK
4 SRQ~
3 EECS
2 ATN~
1 VCC

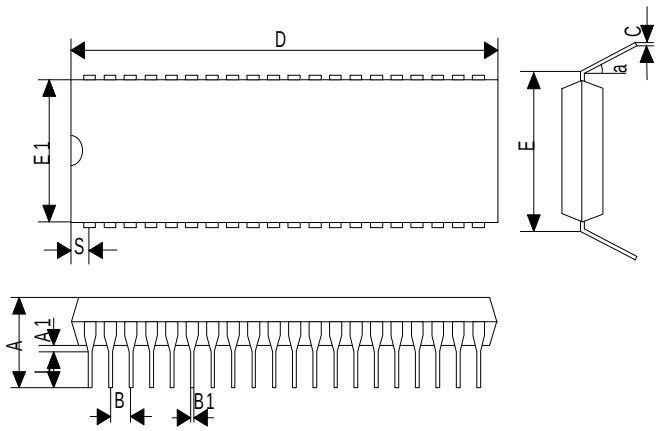

iGPIB
ISA Mode
QFP 80
VCC 41
AT_DRQ 42
AT_SD14 43
AT_DACK~ 44
AT_SD15 45
CS~ 46
AT_IOR~ 47
VCC 48
AT_IOW~ 49
GND 50
CLKOUT 51
AT_IRQ 52
CLKSEL 53
AT_SD0 54
AT_SD1 55
CIC~ 56
AT_SD2 57
AT_SA4 58
AT_SD3 59
GND 60
61 VCC
62 AT_SD4
63 SC
64 AT_SD5
65 SCSEL~
66 AT_SD6
67 AT_SD7
68 DISC
69 GND
70 VCC
71 ISA~
72 AT_SA0
73 DT_R~
74 AT_SA1
75 SE~
76 AT_SA2
77 IFC~
78 AT_SA3
79 REN~
80 GND
40 GND
39 T/R3
38 AT_SD13
37 AT_RESET
36 AT_SD12
35 CLOCK
34 T/R2
33 AT_SD11
32 T/R1
31 PCMCIA~
30 GND
29 VCC
28 AT_SD10
27 EOI~
26 NDAC~
25 AT_SD9
24 NRFD~
23 AT_SD8
22 DAV~
21 GND
20 VCC
19 DIO8~
18 PE
17 DIO7~
16 FIFOTEST~
15 DIO6~
14 DIO5~
13 VCC
12 DIO4~
11 DRV_ENA~
10 GND
9 DIO3~
8 PACK
7 DIO2~
6 DIO1~
5 DB_ENH~
4 SRQ~
3 DB_ENL~
2 ATN~
1 VCC


AT bus connector
i72010
GPIB connector
IRQn
IOW~
IOR~
DACKn~
DRQn
RESET
SD0-15
SA0-9
AT_IRQ~
AT_IOW~
AT_IOR~
AT_DACK~
AT_DRQ
AT_RESET
SD0-15
SA0-4
Address decoder
CS~
CLKSEL
DRVENA
SCSEL~
CLK
DIO~0-7
ATN~
SRQ~
NDAC~
NRFD~
DAV~
IFC~
REN~
EOI~
CLKOUT
CIC~
SC
DT_R~
DB_ENL~
DB_ENH~
T/R1-3
30 MHz Oscillator


PCMCIA connector
i72010
GPIB connector
NIREQ
NIOWR
NOIRD
NWE
NOE
VPP1
NREG
NCE1
NCE2
NINPACK
RESET
PD-7
PA0-9
CLK
CLKSEL
DRVENA
EEDO
EEDI
EECS
EECK
EETYPE
DIO~0-7
ATN~
SRQ~
NDAC~
NRFD~
DAV~
IFC~
REN~
EOI~
PWRDWN
SC
T/R1-3
EEPROM

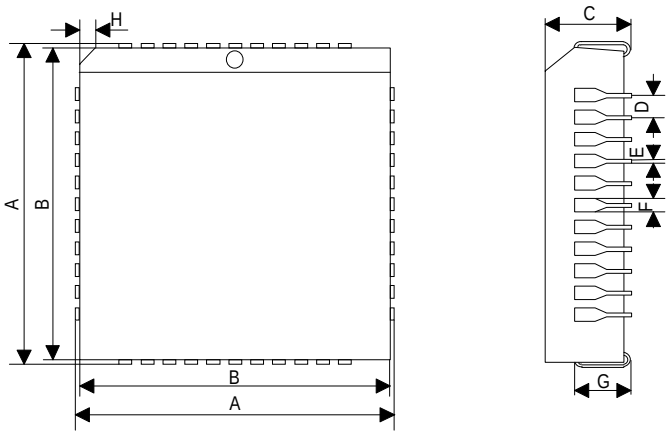
9. Packages

9.1.DIP 40:



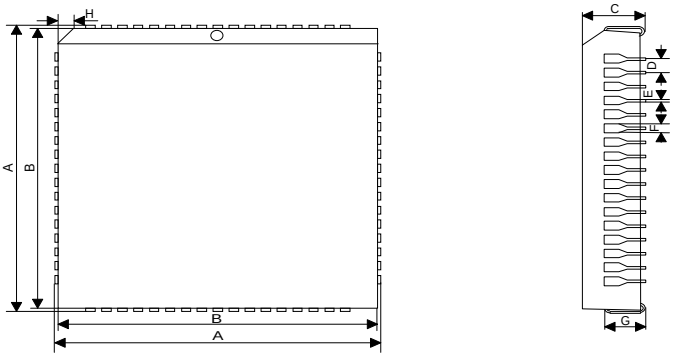
Symbol	min	nom	max
A	-	-	8.77 mm
A1	-	0.38 mm	-
B	-	2.54 mm	-
B1	-	0.46 mm	-
C	-	-	-
D	51.94 mm	52.07 mm	52.20 mm
E	15.24 mm	15.49 mm	15.74 mm
E1	13.84 mm	13.97 mm	14.10 mm
L	-	3.18 mm	-
a	0°	-	15°

9.2.PLCC 44:



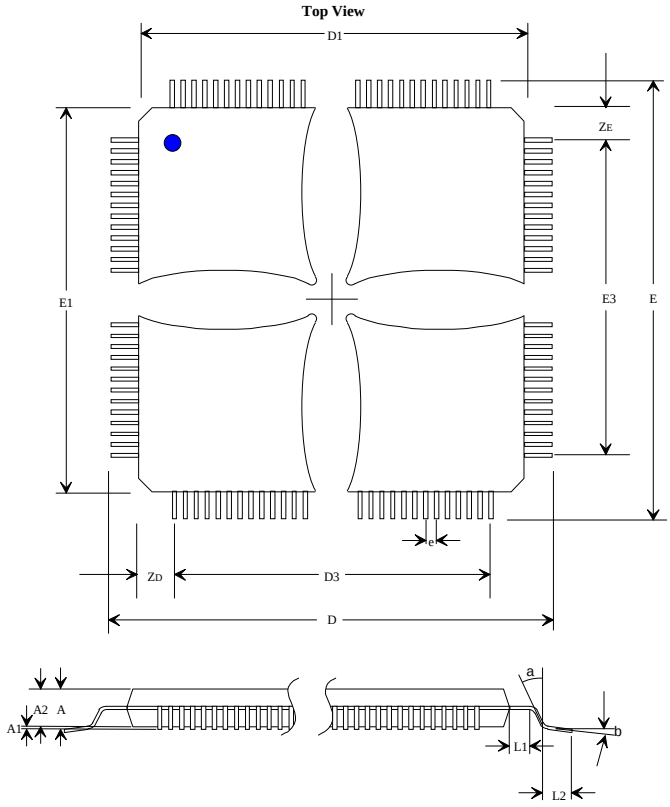
Symbol	min	nom	max
A	17.40 mm	17.52 mm	17.64 mm
B	16,56 mm	16.61 mm	16.66 mm
C	4.32 mm	4.37 mm	4.42 mm
D	1.22 mm	1.27 mm	1.32 mm
E	0.33 mm	0.43 mm	0.53 mm
F	0.67 mm	0.74 mm	0.81 mm
G	2.29 mm	-	3.05 mm
H	-	1.14 mm	-

9.3.PLCC 68:



Symbol	min	nom	max
A	25.03 mm	25.15 mm	25.27 mm
B	24.18 mm	24.23 mm	24.28 mm
C	4.27 mm	4.32 mm	4.37 mm
D	1.22 mm	1.27 mm	1.32 mm
E	0.33 mm	0.43 mm	0.53 mm
F	0.67 mm	0.74 mm	0.67 mm
G	2.29 mm	-	3.30 mm
H	-	1.14 mm	-

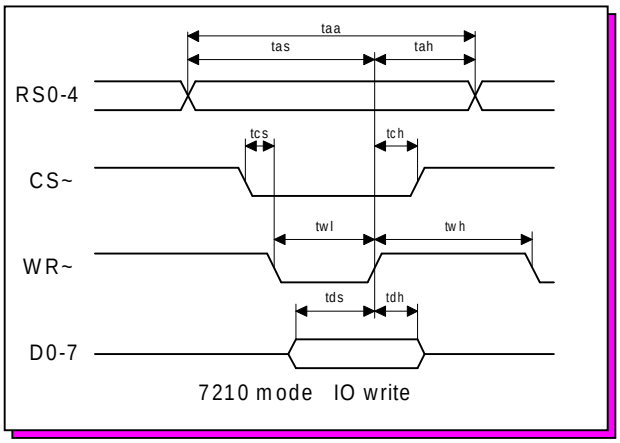
9.4.TQFP80



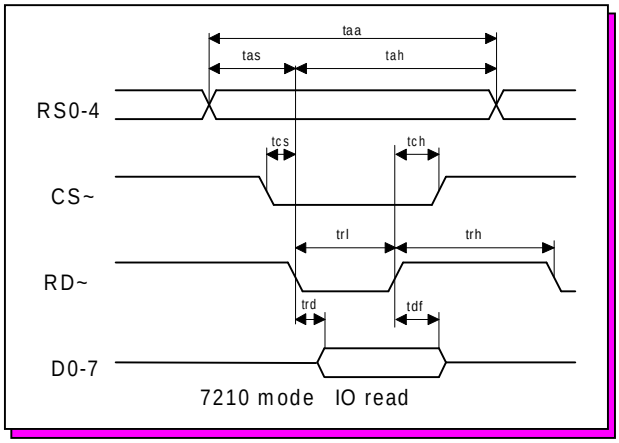
Symbol	min	nom	max
A	-	-	1.20 mm
A1	0.05 mm	-	0.15 mm
A2	0.95 mm	1.00 mm	1.05 mm
D	-	14.00 mm	±0.2 mm
D1	-	12.00 mm	±0.1 mm
E	-	14.00 mm	±0.2 mm
E1	-	12.00 mm	±0.1 mm
e	-	0.50 mm	-
L1	0.20 mm	-	-
L2	0.45 mm	0.60 mm	0.75 mm
N	-	80.00 mm	-
a	0°	-	-
b	0°	7°	-

10. Timings

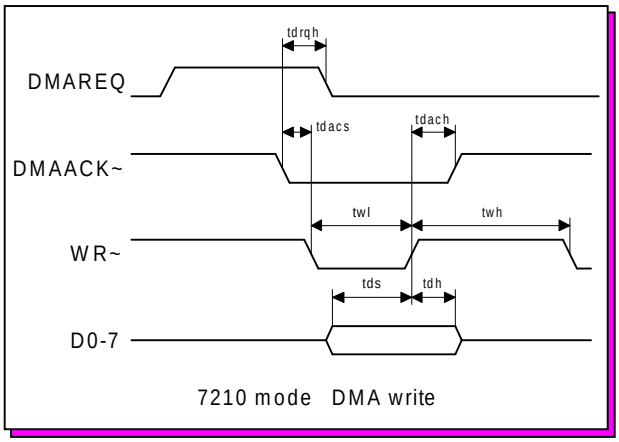
10.1.Timings for 7210 compatible mode:



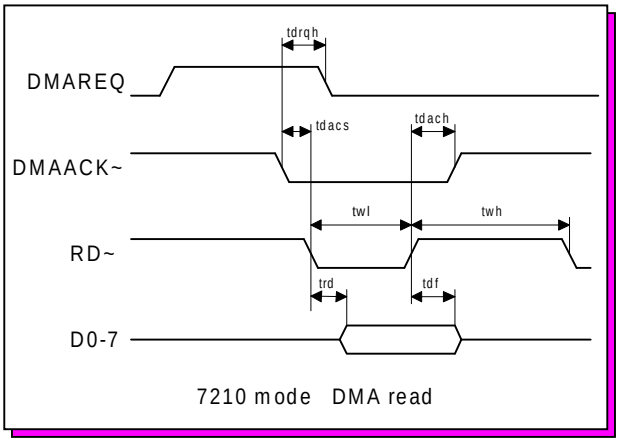
7210 mode IO write



7210 mode IO read

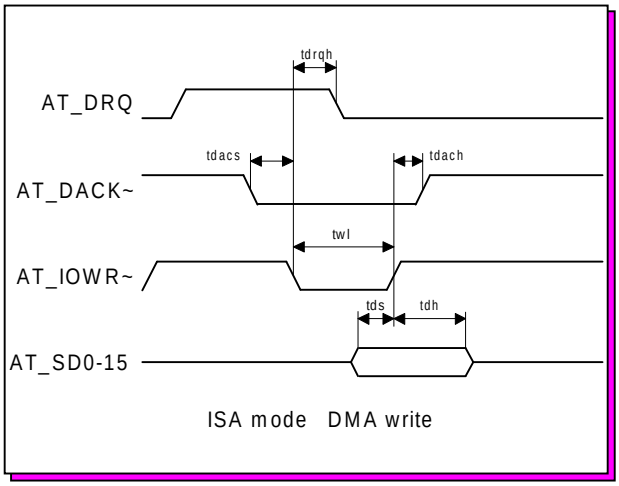


7210 mode DMA write

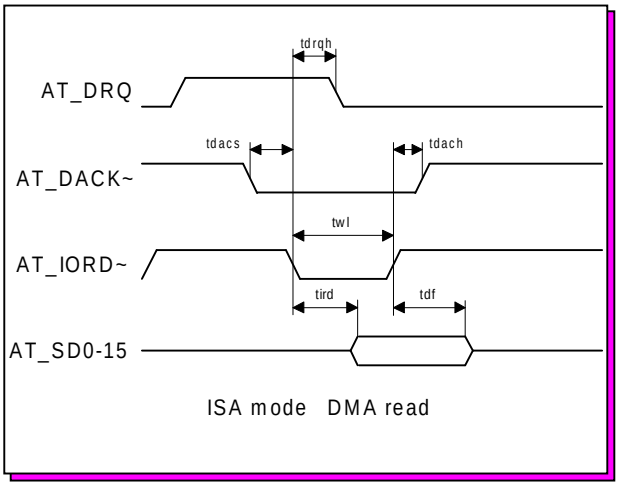


7210 mode DMA read

10.2.Timings for ISA DMA mode:

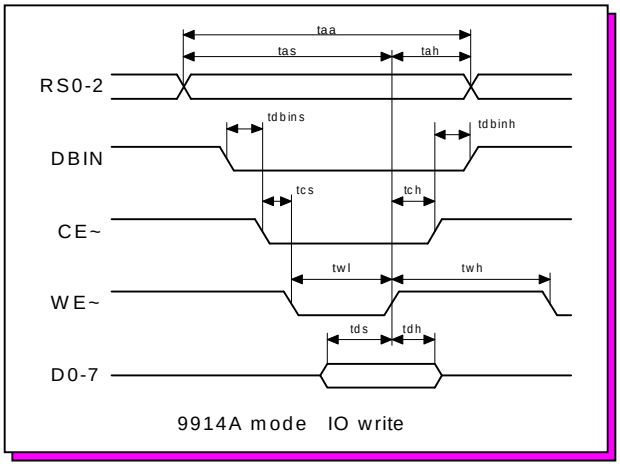


ISA mode DMA write

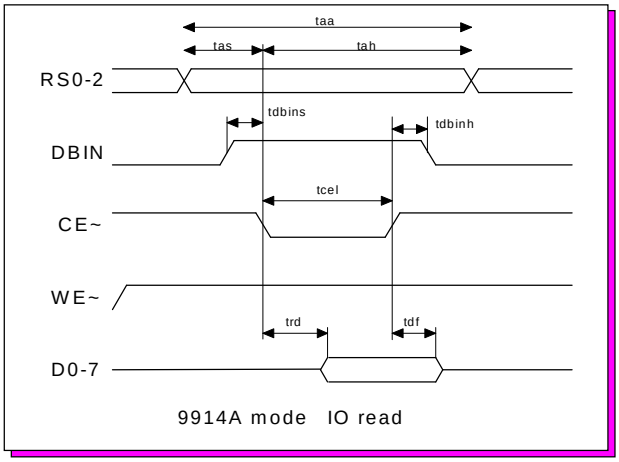


ISA mode DMA read

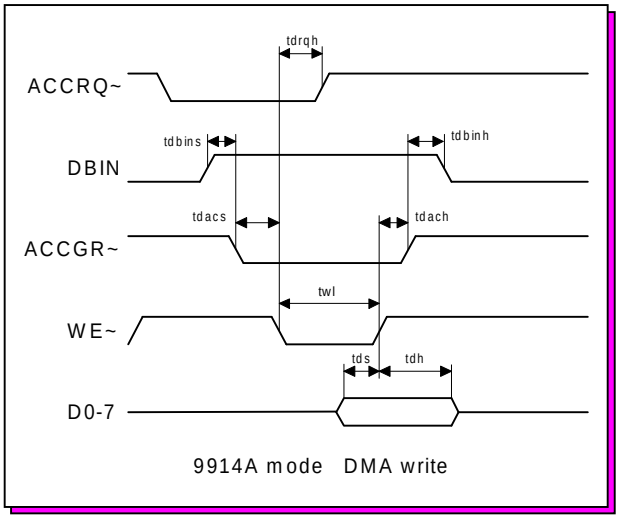
10.3.Timings for 9914A compatible mode:



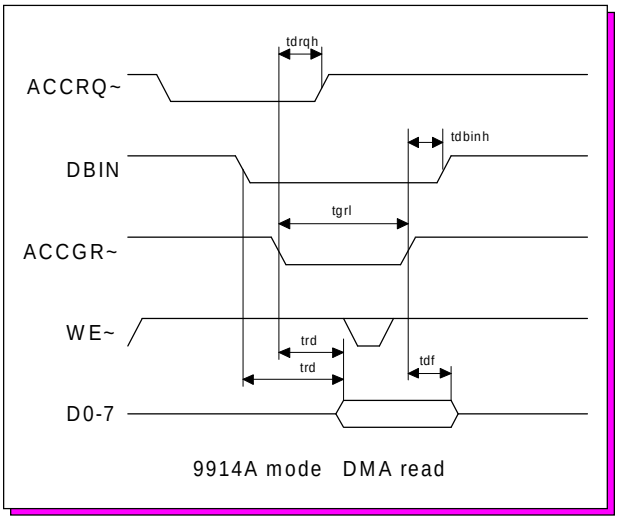
9914A mode IO write



9914A mode IO read



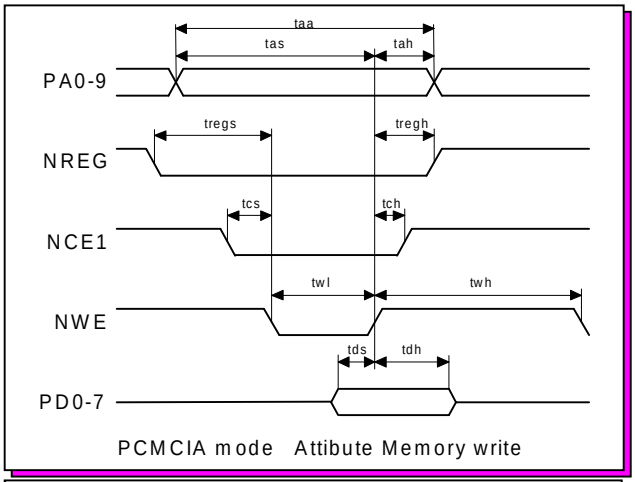
9914A mode DMA write



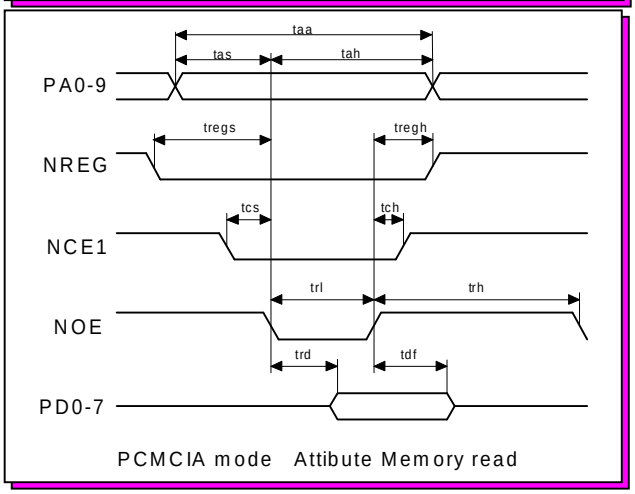
9914A mode DMA read

Note: During DMA read access a WE~ low impulse may occur.

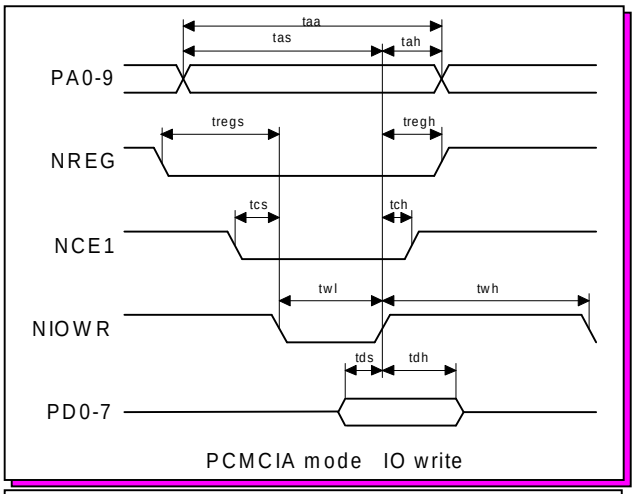
10.4.Timings for PCMCIA interface mode:



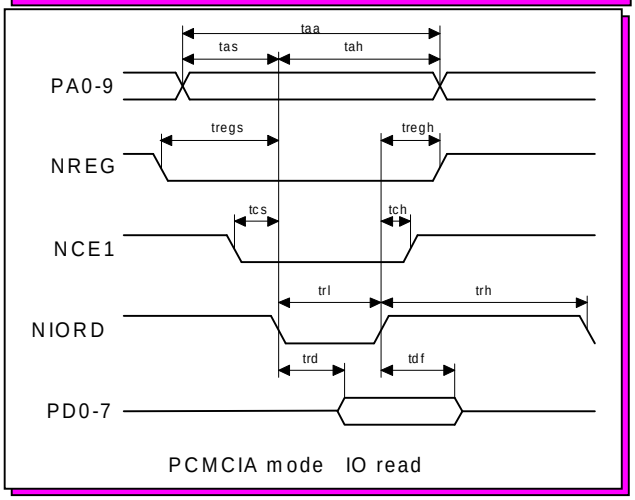
PCMCIA mode Attibute Memory write



PCMCIA mode Attibute Memory read

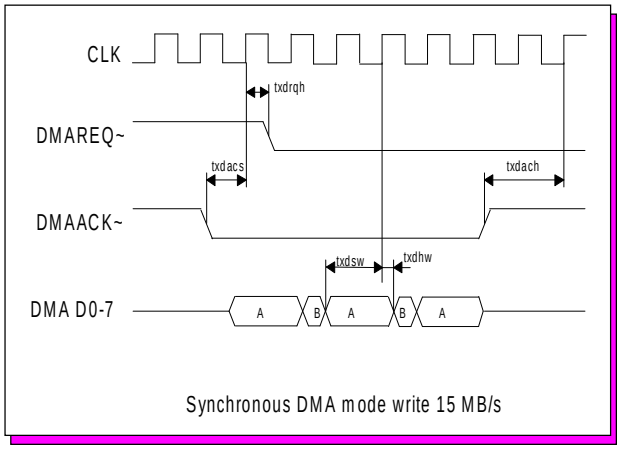


PCMCIA mode IO write

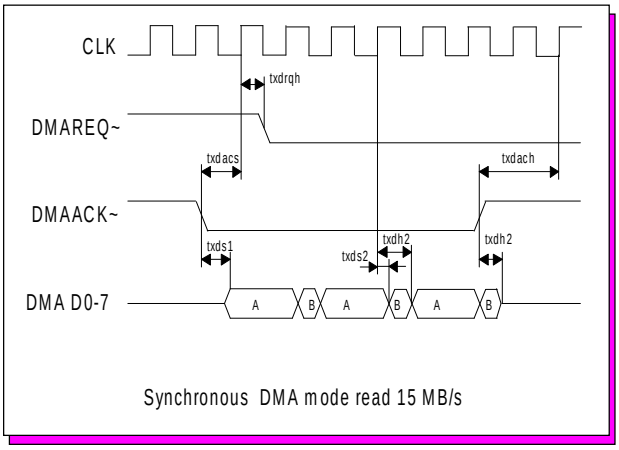


PCMCIA mode IO read

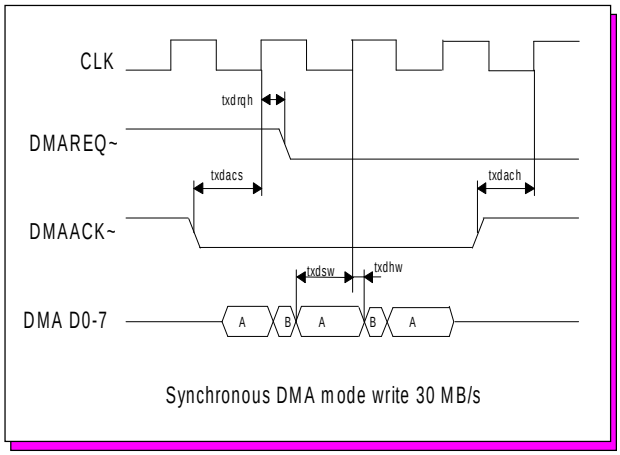
10.5.Timing for synchronous DMA interface:



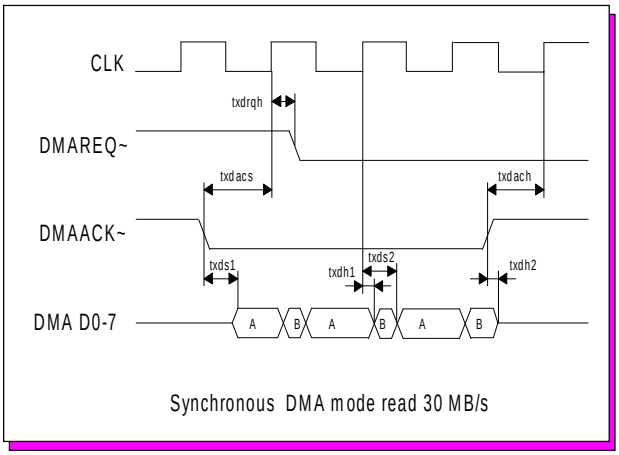
Synchronous DMA mode write 15 MB/s



Synchronous DMA mode read 15 MB/s



Synchronous DMA mode write 30 MB/s



Synchronous DMA mode read 30 MB/s

Note: A marks valid date, B marks invalid data.

10.6.Timing Value Table

Symbol	Description	Time in ns	Time in ns
		min	max
tas	address setup time	0	
tah	address hold time	35	
taa	address active time	70	
tcs	chip select setup time	0	
tch	chip select hold time	0	
twl	write low time	70	
twh	write high time	70	
trl	read low time	70	
trh	read high time	70	
tds	data setup time	70	
tdh	data hold time	0	
trd	data read delay time		~90
tdf	data to float time		~70
tdrqh	dma request hold time		~100
tdacs	dma ack setup time	0	
tdach	dma ack hold time	0	
tdbins	dbin setup time	0	
tdbinh	dbin hold time	0	
tgrl	DMA grand low time	70	
tcel	chip enable low time	70	
tregs	nreg setup time	0	
tregh	nreg hold time	0	
tird	isa dma read to data time		~130
txdrqh	xdma request hold time		max. 30
txdacs	xdma acknowledge setup time	0	
txdach	xdma acknowledge hold time	0	
txds1	xdma first data setup time		max. 30
txds2	xdma following data setup time		max. 30
txdh1	xdma data hold time		max. 30
txdh2	xdma last data to fload time		max. 30
txdsw	xdma data write setup time	0	
txdhw	xdma data write hold time	max. 30	

11. Power and Temperature Ratings

11.1 Absolute maximum ratings
Stresses beyond those listed in table may cause permanent damage to the circuit. The functional operation is made sure only within the limits of the 'Recommended operating conditions'. Exposure to absolute maximum rating condition for extended periods may affect reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_S	-40	125	°C
Operating Temperature	T_O	-40	85	°C
ESD-Protection		-2	2	kV
Supply Voltages	V_{DD}	-0.3	7	V
In- and output Voltages	V_{IN}	-0.3	V_{DD}+0.3V	V

11.2 Recommended operating conditions

Parameter	Symbol	Min	Max	Unit
Junction Temperature	T_J		150	°C
Ambient Temperature	T_A	-40	85	°C
Supply Voltage	V_{DD}	4.5	5.5	V

11.3 GPIB Bus Transceivers / Line drivers
The specifications of the line drivers follow the recommendations of the IEEE488.1 / IEC60625.1 standard.

11.4 DC-Characteristics

Parameter	Symbol	Min	Max	Unit	Remark
Average supply current	I_{AS}		200	mA	with GPIB line drivers off
All digital inputs and outputs					
Input Capacitance			20	pF	
Input Leakage Current		-10	10	µA	
Output Leakage Current		-10	10	µA	
Schmitt-Trigger Inputs 5V (TTL)					
High-Level InputVoltage	V_{IH}	2.0		V	
Low-Level InputVoltage	V_{IL}		0.8	V	
CMOS Outputs 5V/6mA					
High-Level Output Voltage	V_{QH}	2.4		V	I_{QH} = -2 mA
Low-Level Output Voltage	V_{QL}		0.4	V	I_{QL} = 2 mA
CMOS Outputs 5V/24mA					
High-Level Output Voltage	V_{QH}	2.4		V	I_{QH} = -8 mA
Low-Level Output Voltage	V_{QL}		0.4	V	I_{QL} = 8 mA
Clock					
Clock Frequency	f		30	MHz	external Clock
	f		8,4,2,1[1]	MHz	NEC uPD7210 compatible
	f		5-4,2,1[1]	MHz	TI TMS9914A compatible

[1] Selected chips must be ordered. Please specify desired clock frequency in order.